CHAPTER 7

Differential and Multistage Amplifiers

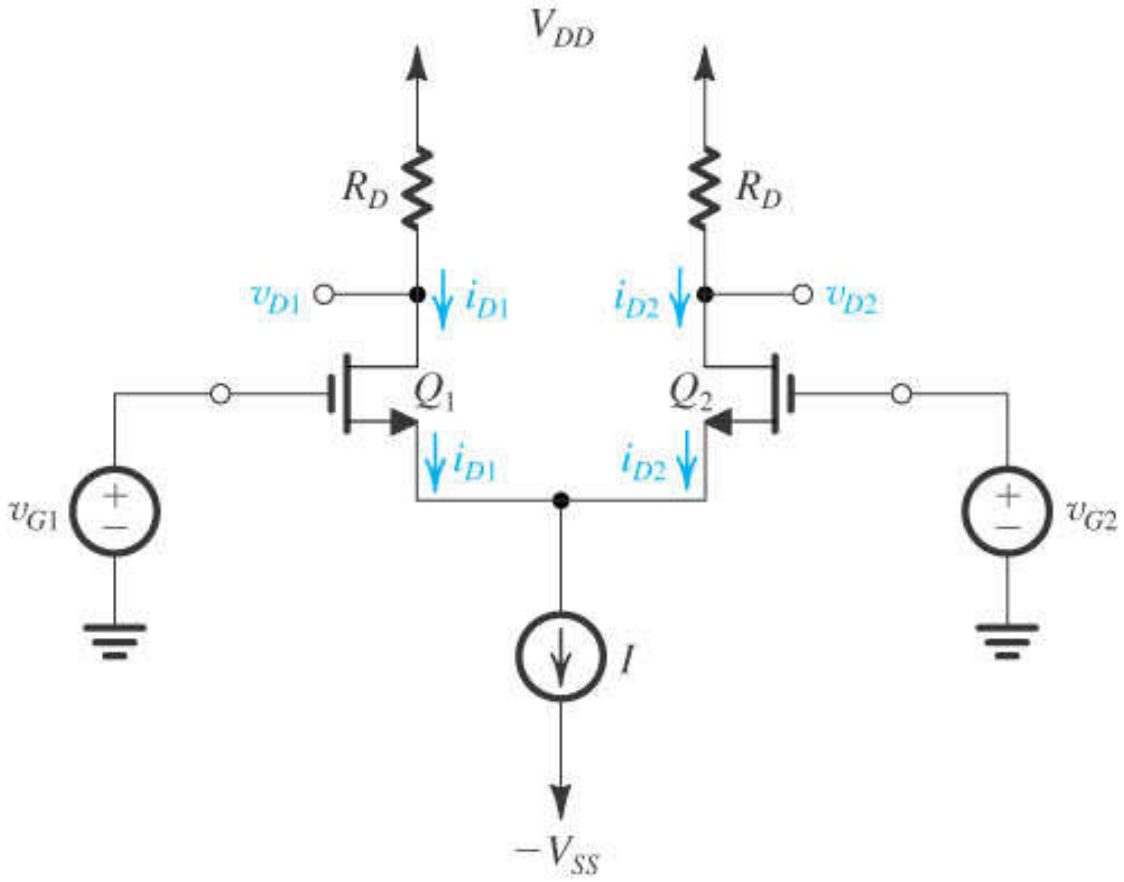

Figure 7.1 The basic MOS differential-pair configuration.

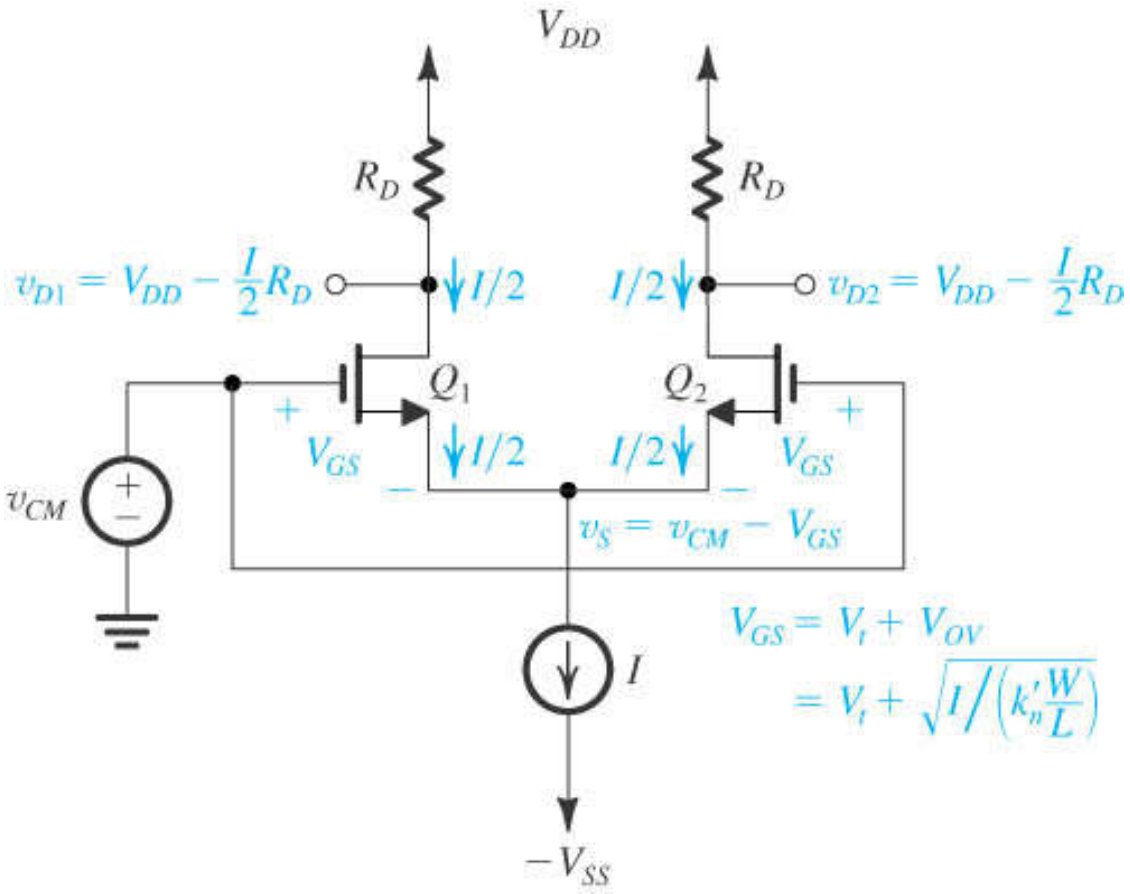

Figure 7.2 The MOS differential pair with a common-mode input voltage v_{CM}.

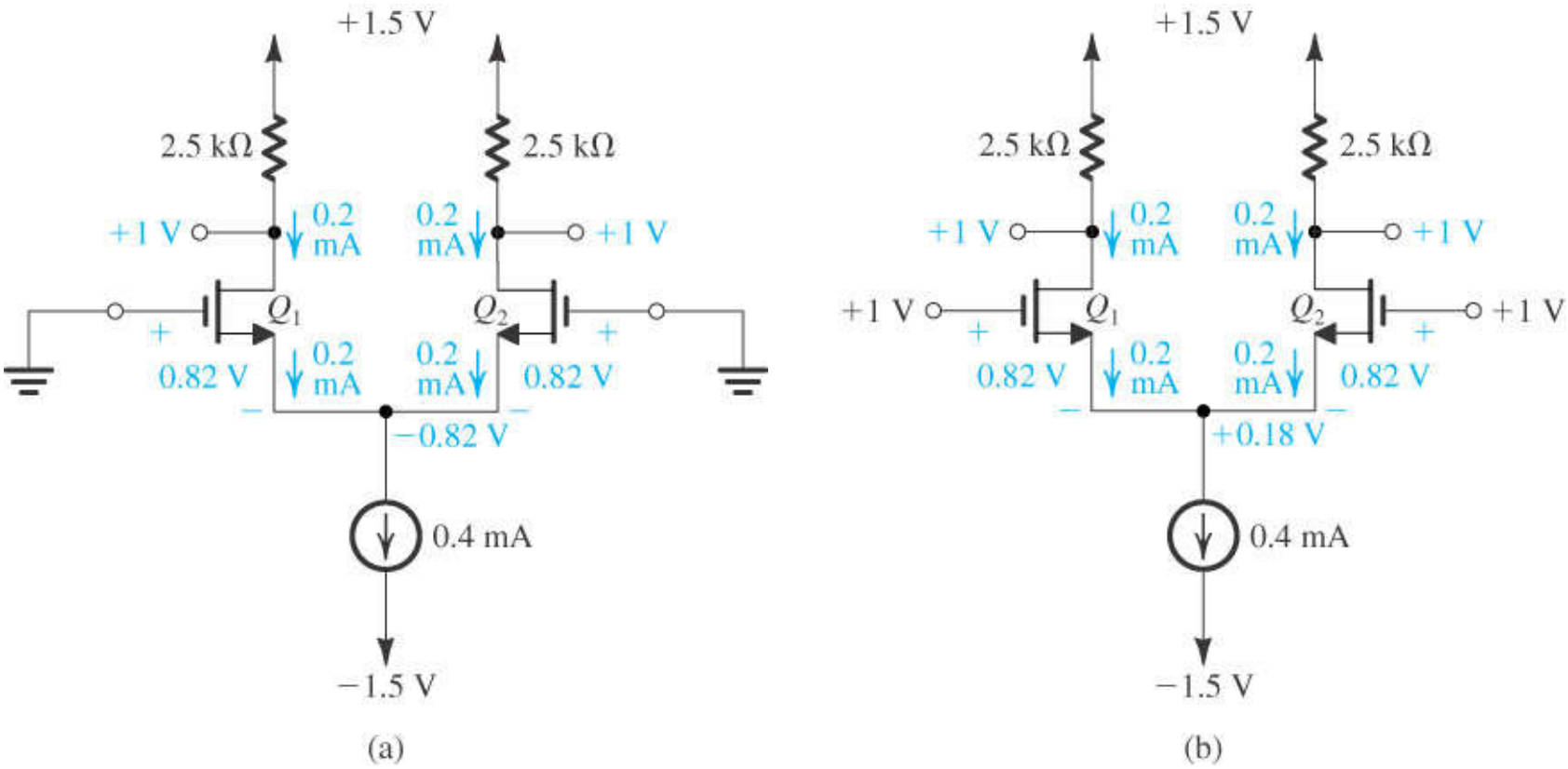

Figure 7.3 Circuits for Exercise 7.1. Effects of varying v_{CM} on the operation of the differential pair.

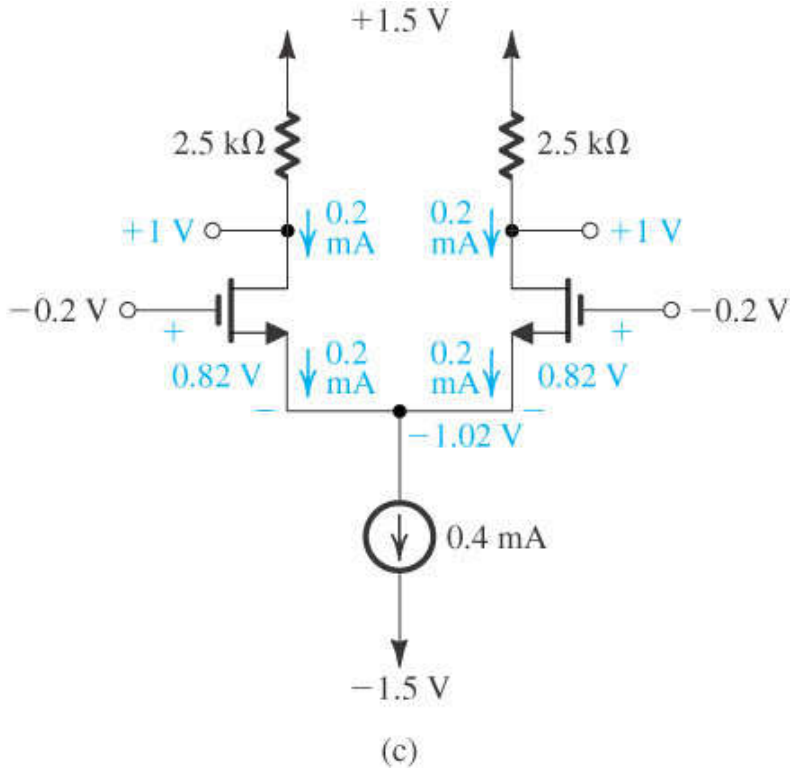

Figure 7.3 *(Continued)*

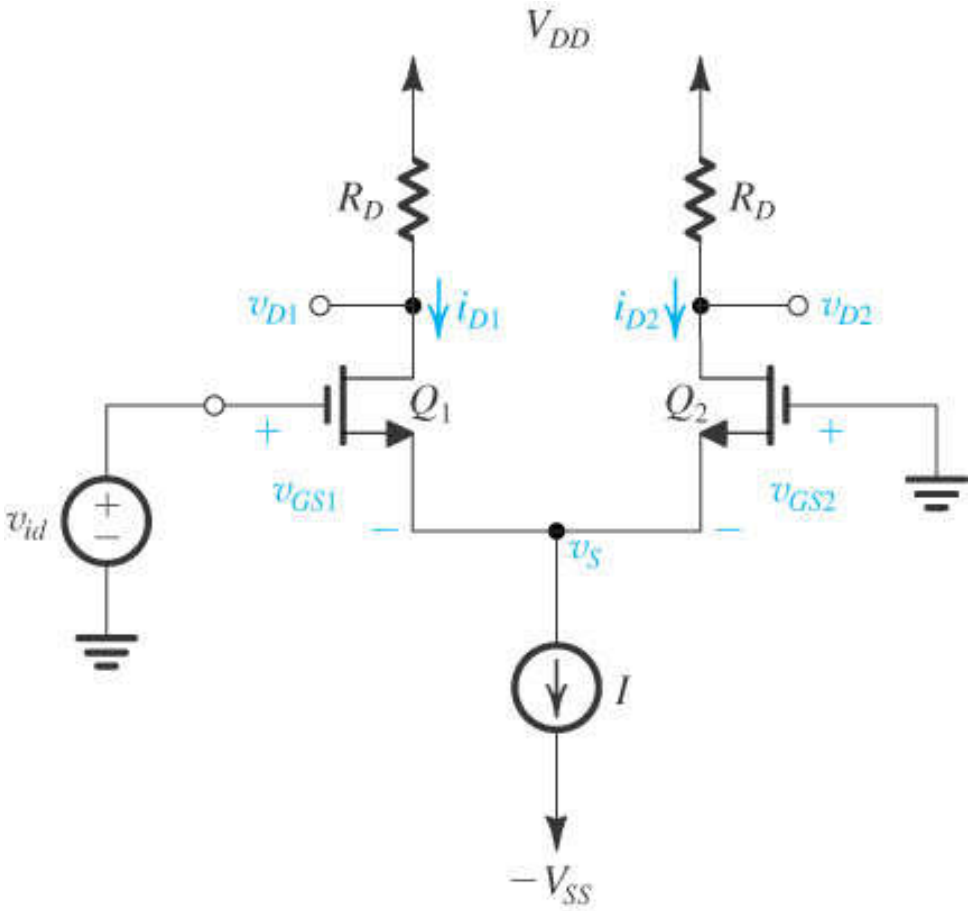

Figure 7.4 The MOS differential pair with a differential input signal v_{id} applied. With v_{id} positive: $v_{GS1} > v_{GS2}$, $i_{D1} > i_{D2}$, and $v_{D1} < v_{D2}$; thus $(v_{D2} - v_{D1})$ will be positive. With v_{id} negative: $v_{GS1} < v_{GS2}$, $i_{D1} < i_{D2}$, and $v_{D1} > v_{D2}$; thus $(v_{D2} - v_{D1})$ will be negative.

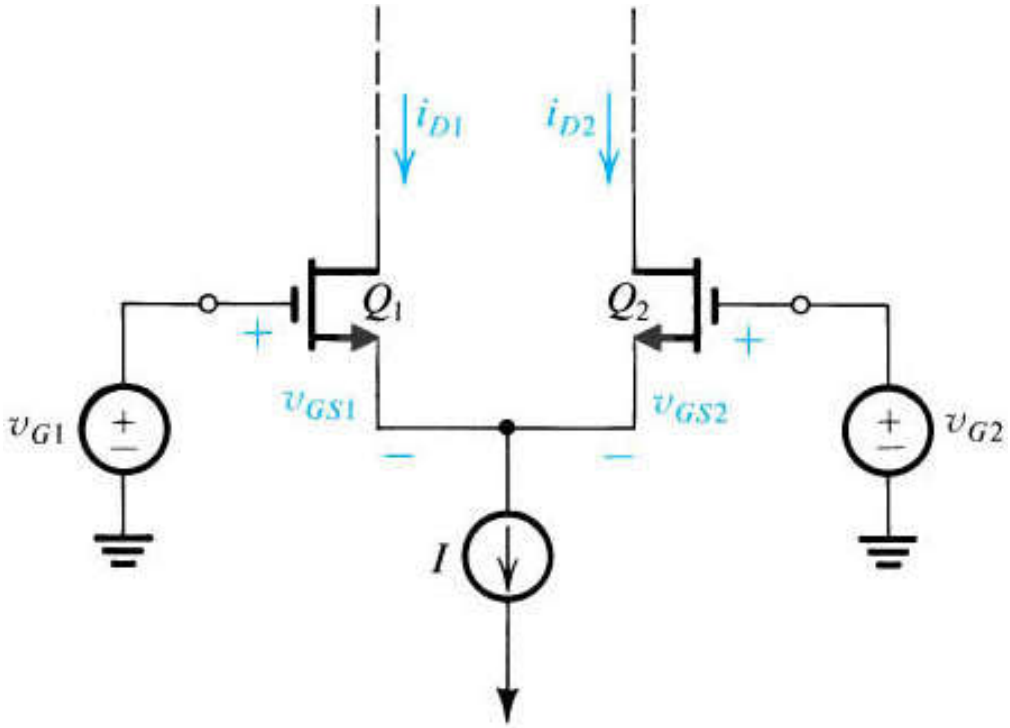

Figure 7.5 The MOSFET differential pair for the purpose of deriving the transfer characteristics, i_{D1} and i_{D2} versus $v_{id} = v_{G1} - v_{G2}$.

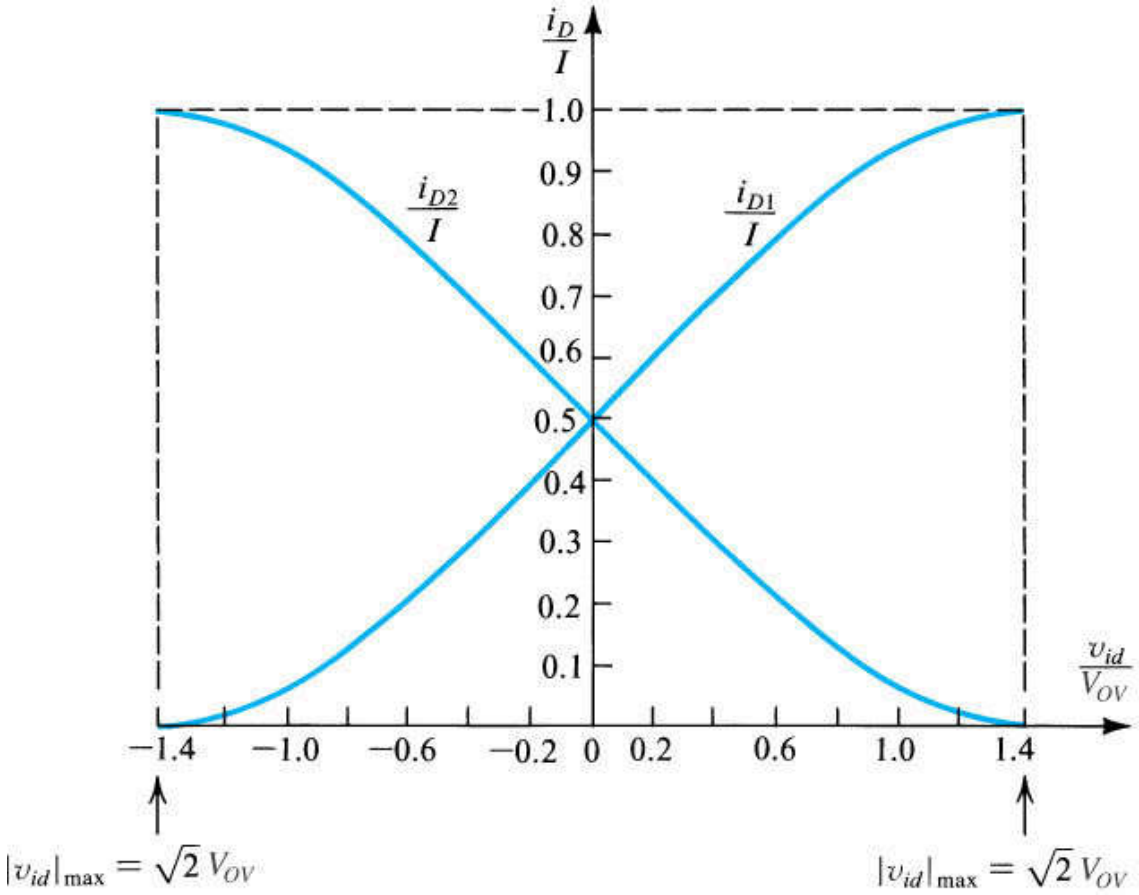

Figure 7.6 Normalized plots of the currents in a MOSFET differential pair. Note that V_{OV} is the overdrive voltage at which Q_1 and Q_2 operate when conducting drain currents equal to $I/2$.

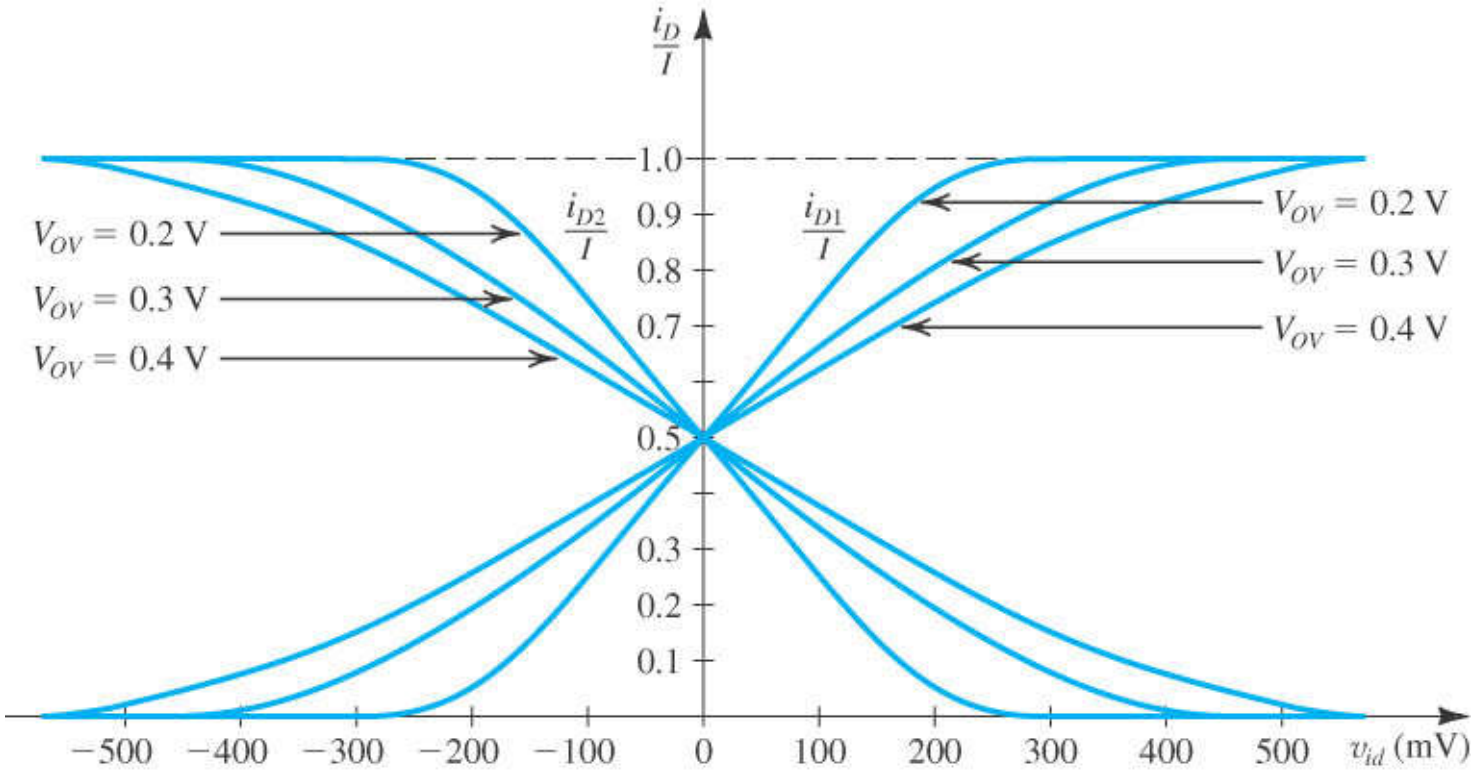

Figure 7.7 The linear range of operation of the MOS differential pair can be extended by operating the transistor at a higher value of V_{OV}.

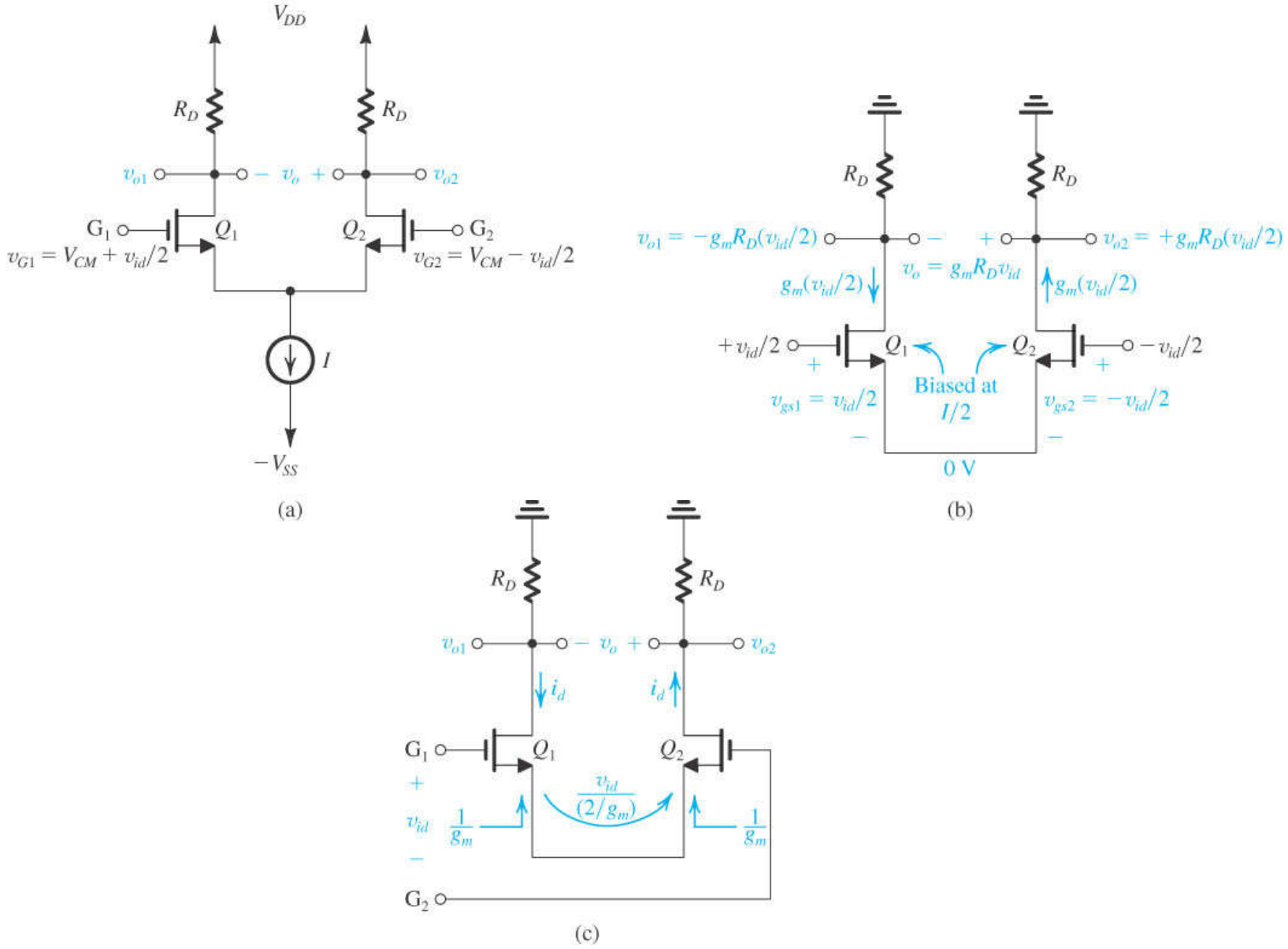

Figure 7.8 Small-signal analysis of the MOS differential amplifier: **(a)** The circuit with a common-mode voltage applied to set the dc bias voltage at the gates and with v_{id} applied in a complementary (or balanced) manner. **(b)** The circuit prepared for small-signal analysis. **(c)** An alternative way of looking at the small-signal operation of the circuit.

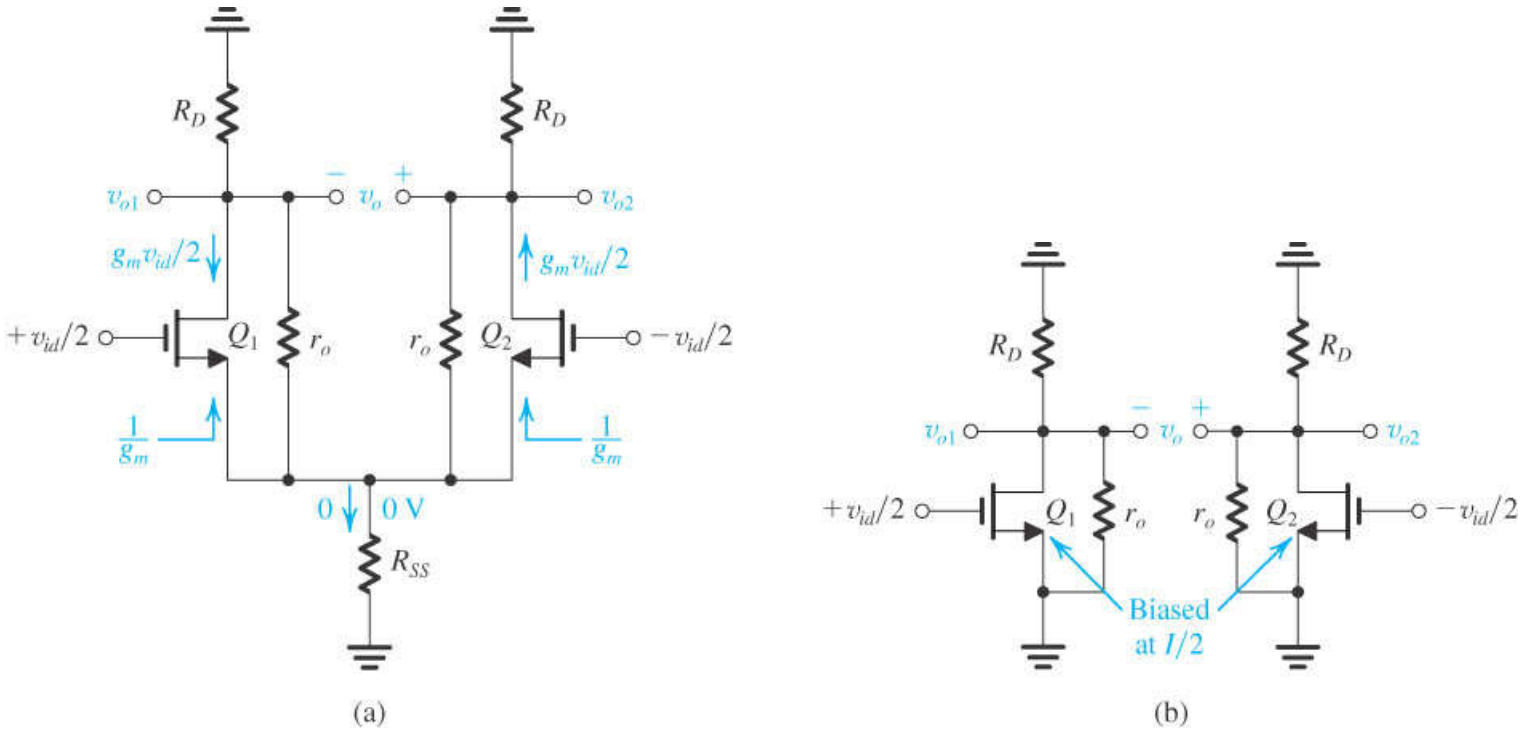

Figure 7.9 **(a)** MOS differential amplifier with r_o and R_{SS} taken into account. **(b)** Equivalent circuit for determining the differential gain. Each of the two halves of the differential amplifier circuit is a common-source amplifier, known as its differential "half-circuit."

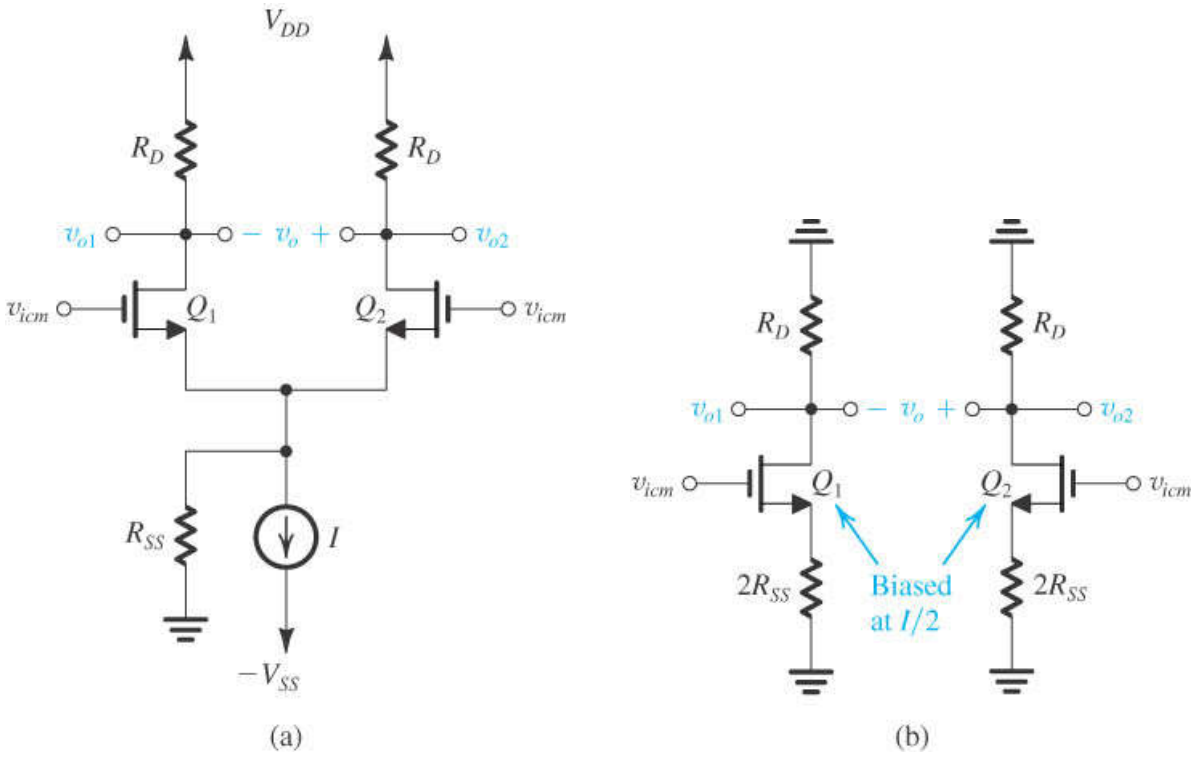

Figure 7.10 **(a)** The MOS differential amplifier with a common-mode input signal v_{icm}. **(b)** Equivalent circuit for determining the common-mode gain (with r_o ignored). Each half of the circuit is known as the "common-mode half-circuit."

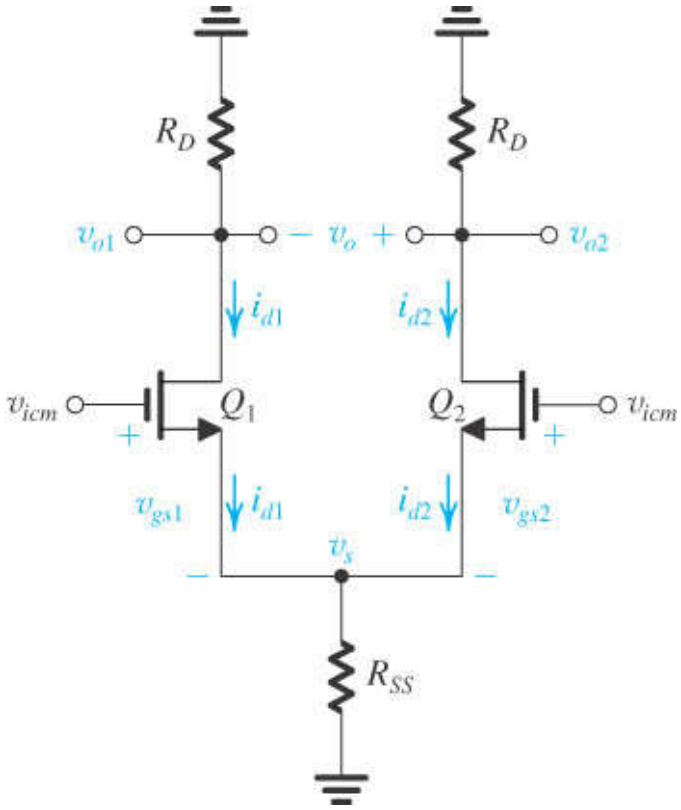

Figure 7.11 Analysis of the MOS differential amplifier to determine the common-mode gain resulting from a mismatch in the g_m values of Q_1 and Q_2.

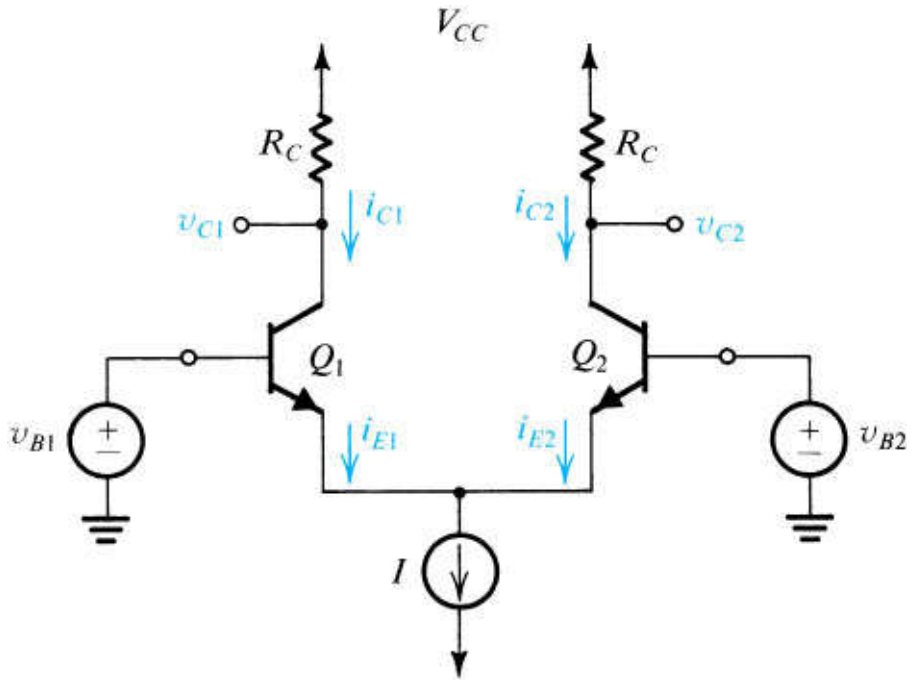

Figure 7.12 The basic BJT differential-pair configuration.

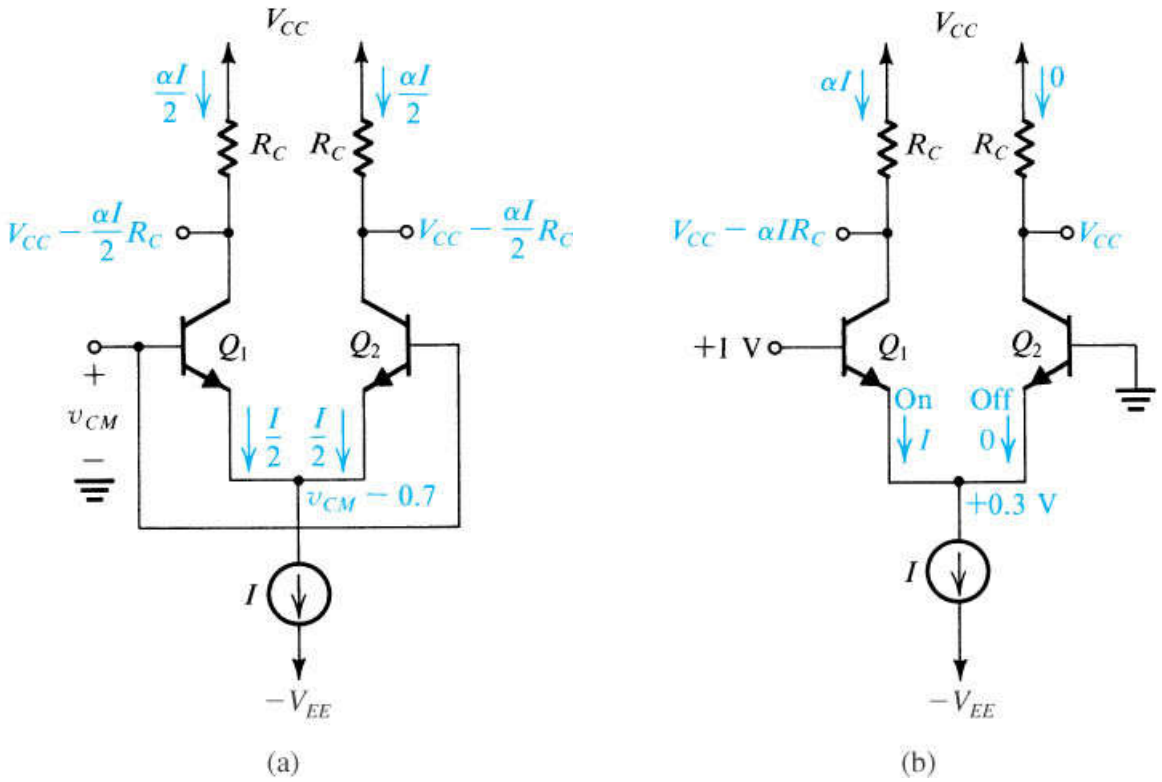

Figure 7.13 Different modes of operation of the BJT differential pair: **(a)** The differential pair with a common-mode input signal v_{CM}. **(b)** The differential pair with a "large" differential input signal.

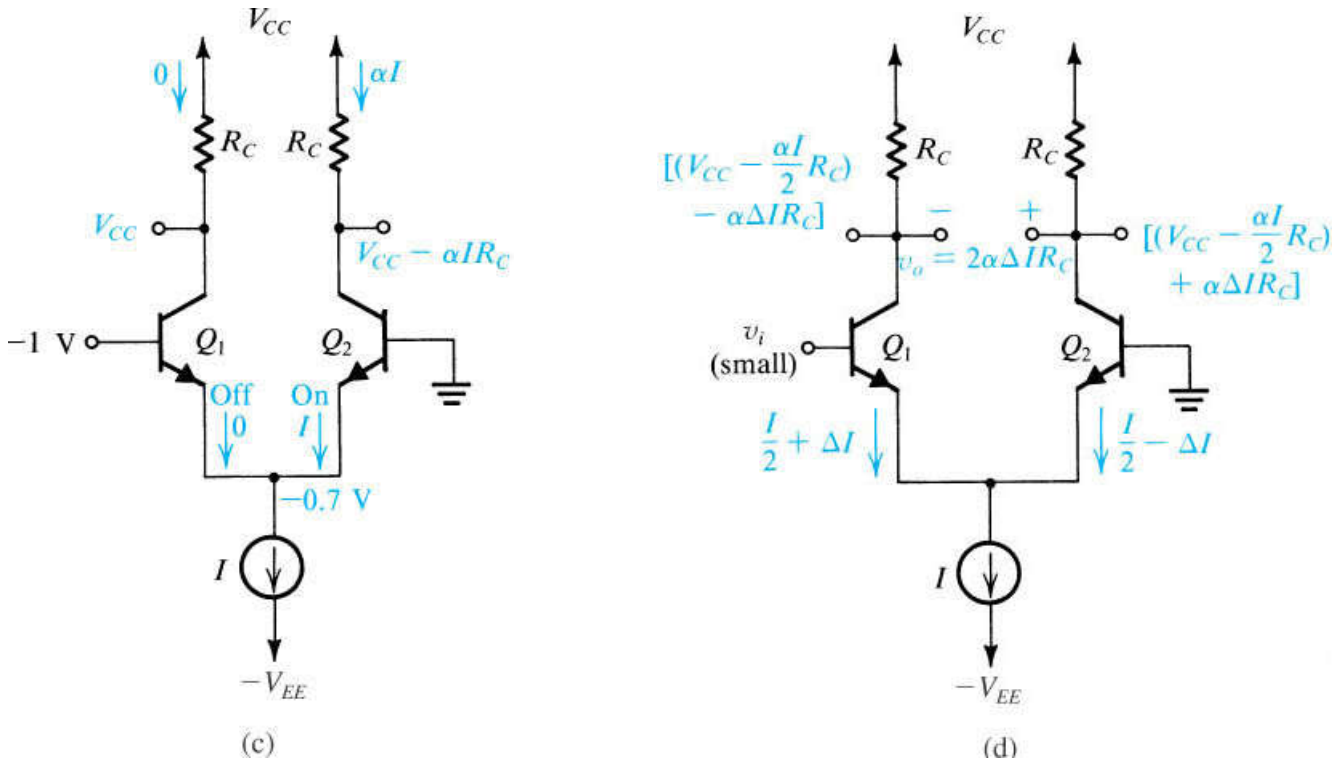

Figure 7.13 *(Continued)* **(c)** The differential pair with a large differential input signal of polarity opposite to that in (b). **(d)** The differential pair with a small differential input signal v_i. Note that we have assumed the bias current source I to be ideal (i.e., it has an infinite output resistance) and thus I remains constant with the change in v_{CM}.

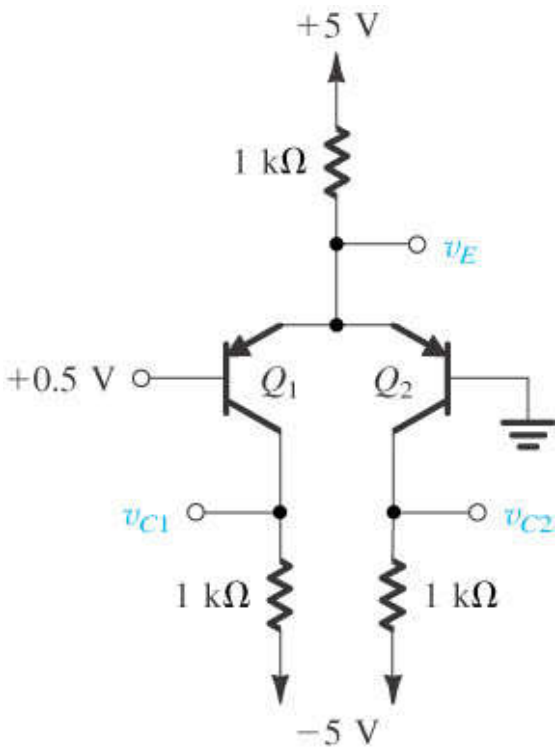

Figure E7.7

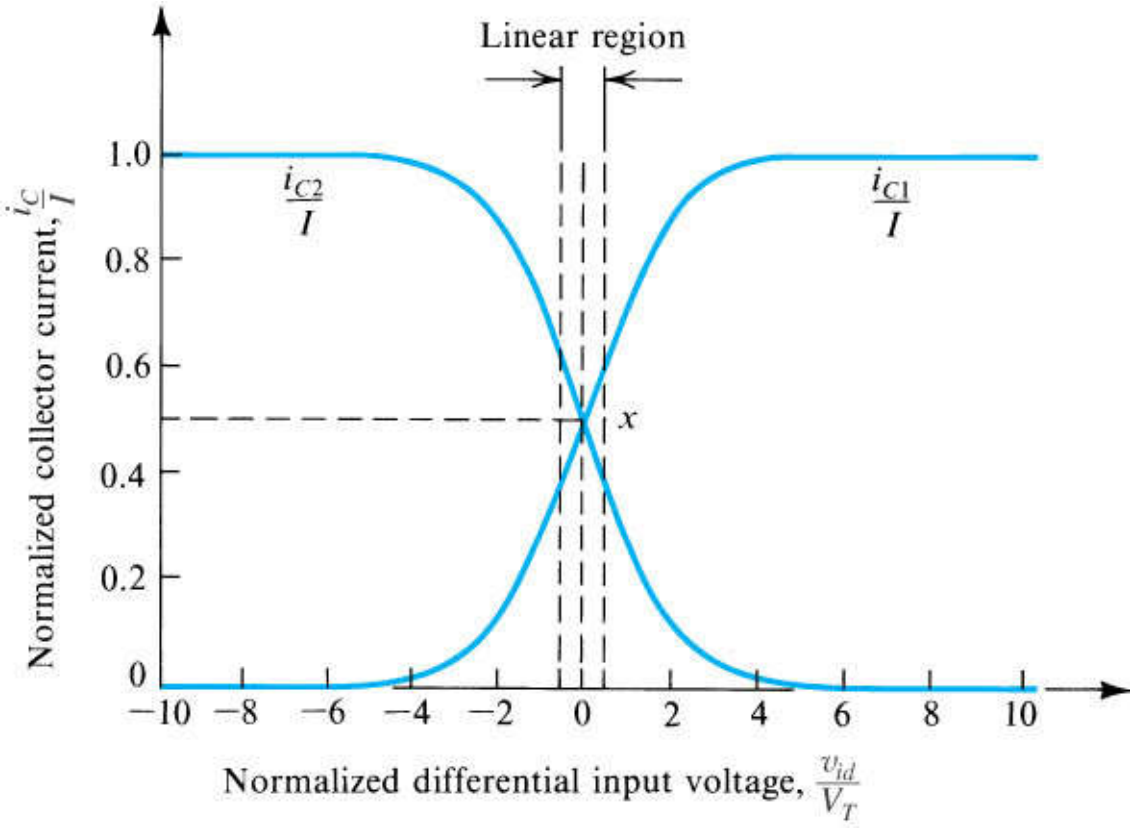

Figure 7.14 Transfer characteristics of the BJT differential pair of Fig. 7.12 assuming α . 1.

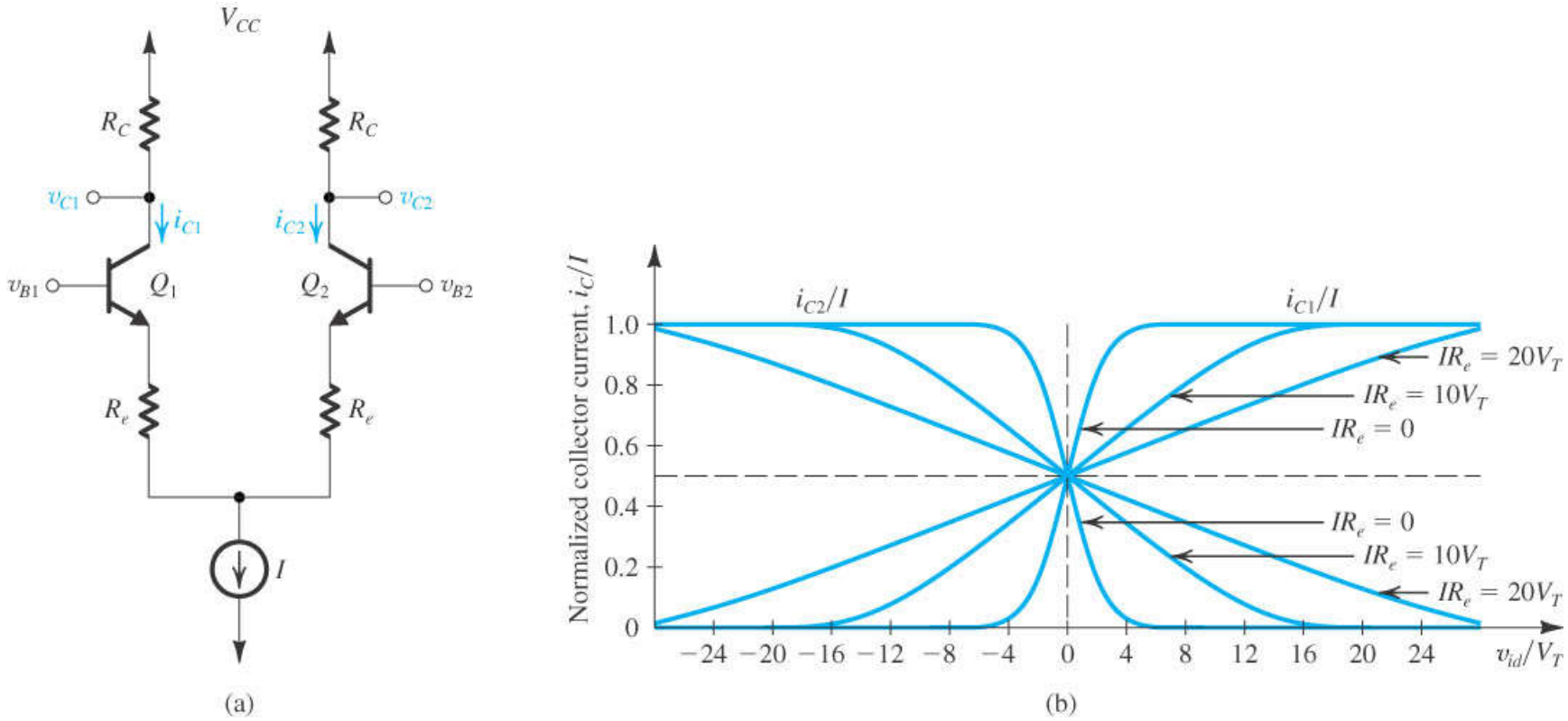

Figure 7.15 The transfer characteristics of the BJT differential pair **(a)** can be linearized **(b)** (i.e., the linear range of operation can be extended) by including resistances in the emitters.

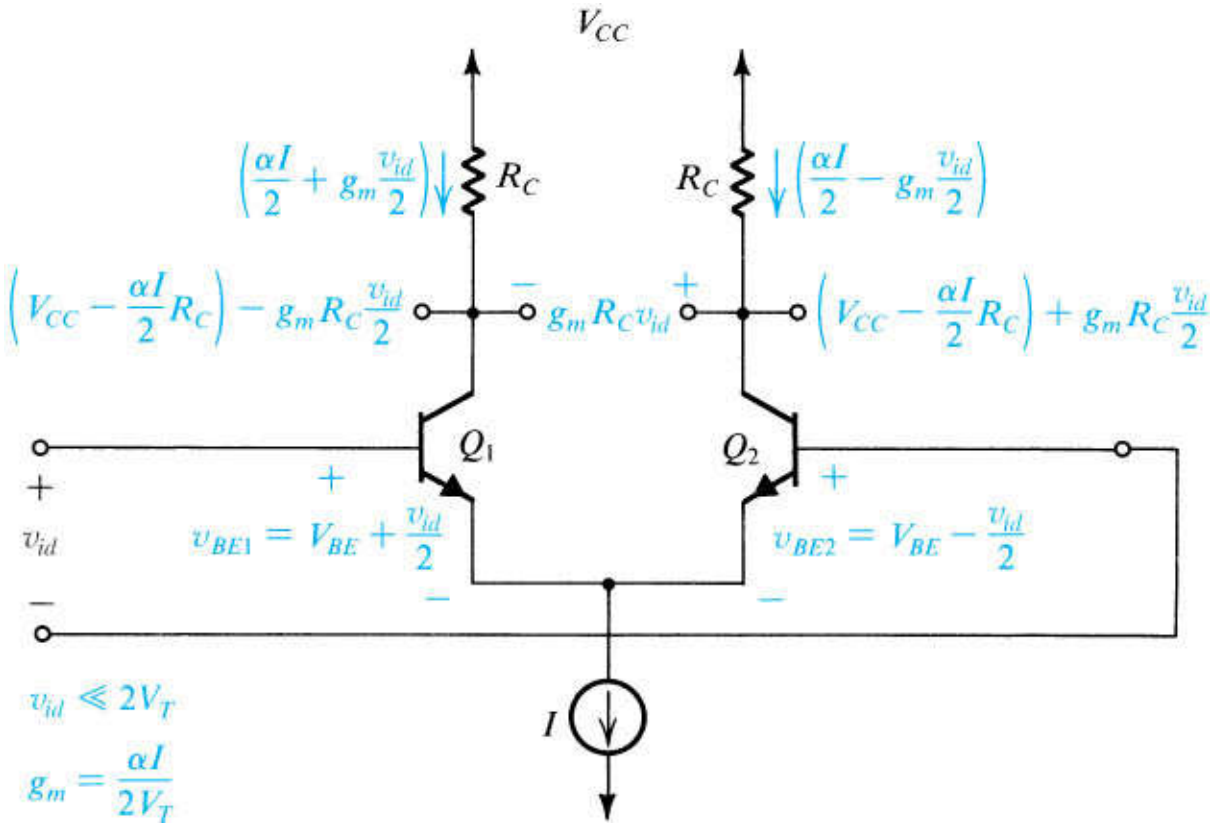

Figure 7.16 The currents and voltages in the differential amplifier when a small differential input signal v_{id} is applied.

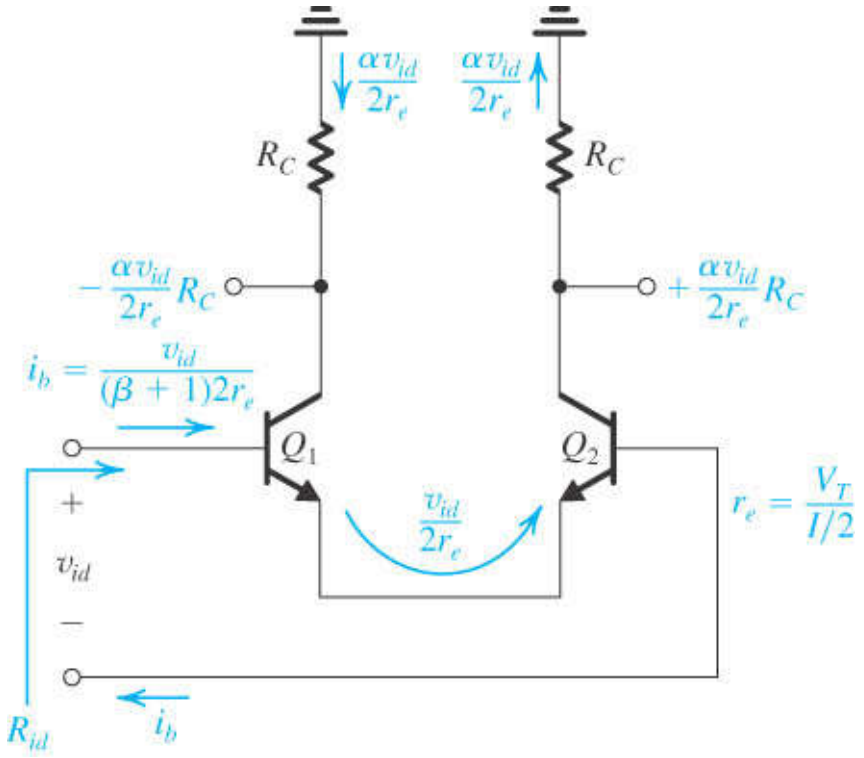

Figure 7.17 A simple technique for determining the signal currents in a differential amplifier excited by a differential voltage signal v_{id}; dc quantities are not shown.

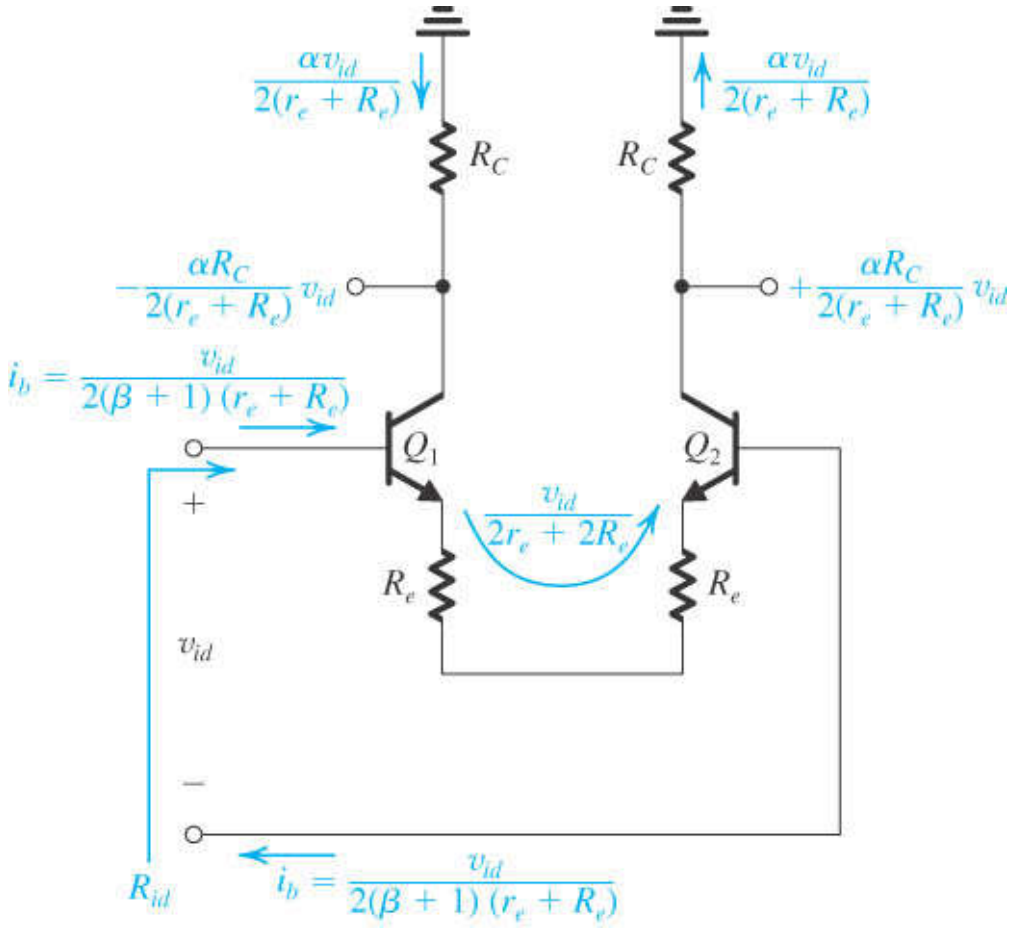

Figure 7.18 A differential amplifier with emitter resistances. Only signal quantities are shown (in color).

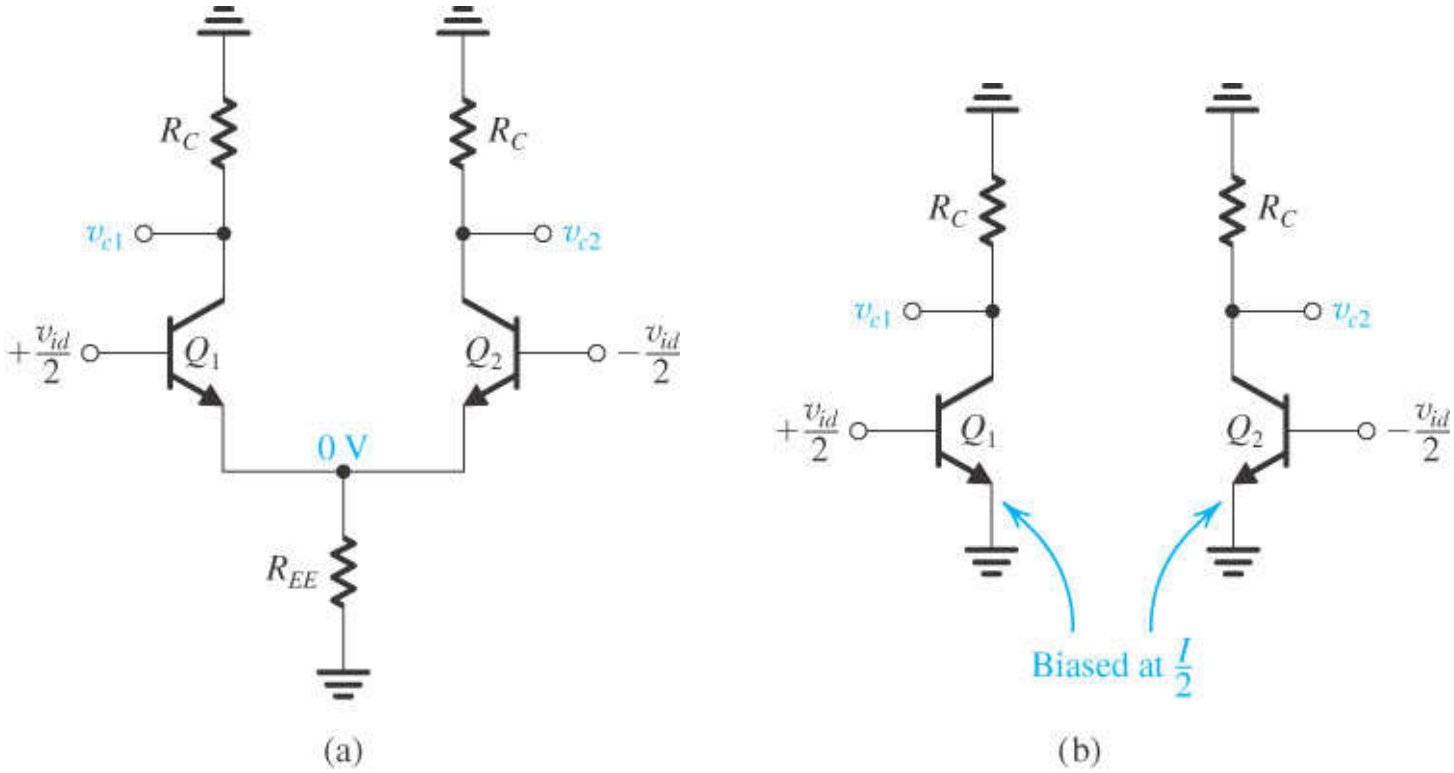

Figure 7.19 Equivalence of the BJT differential amplifier in **(a)** to the two common-emitter amplifiers in (b). This equivalence applies only for differential input signals. Either of the two common-emitter amplifiers in **(b)** can be used to find the differential gain, differential input resistance, frequency response, and so on, of the differential amplifier.

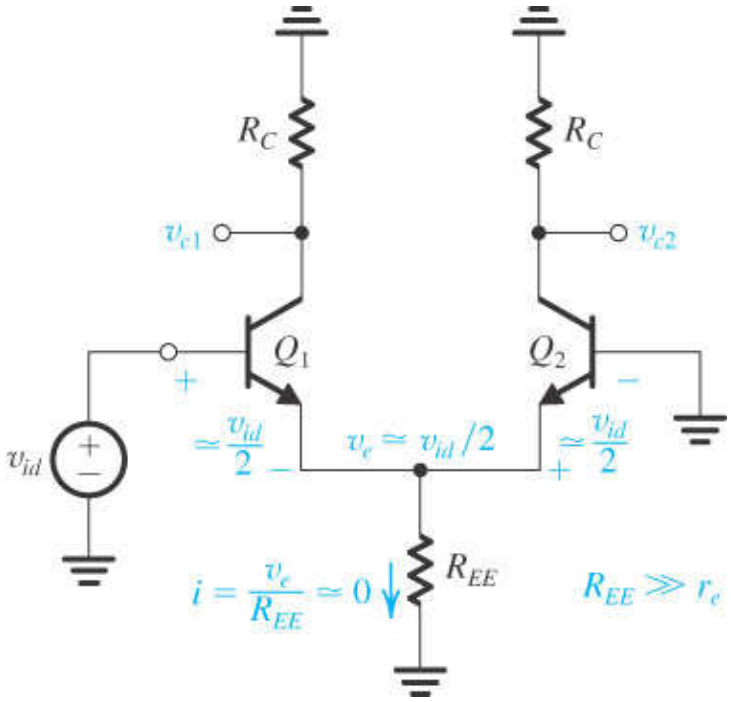

Figure 7.20 The differential amplifier fed in a single-ended fashion.

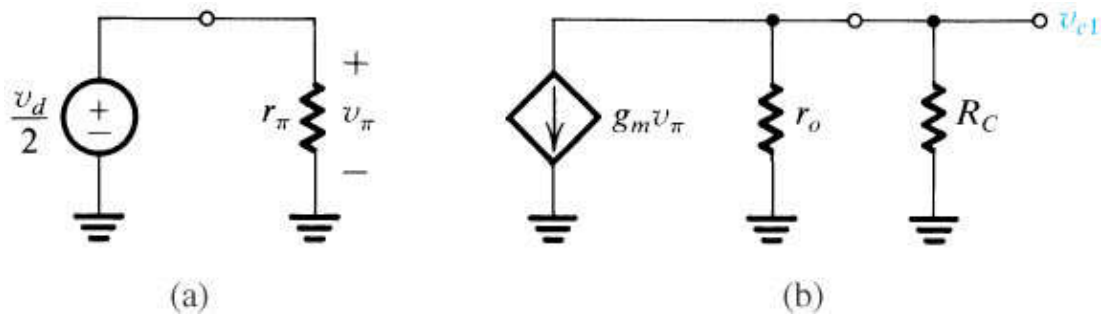

Figure 7.21 **(a)** The differential half-circuit and **(b)** its equivalent circuit model.

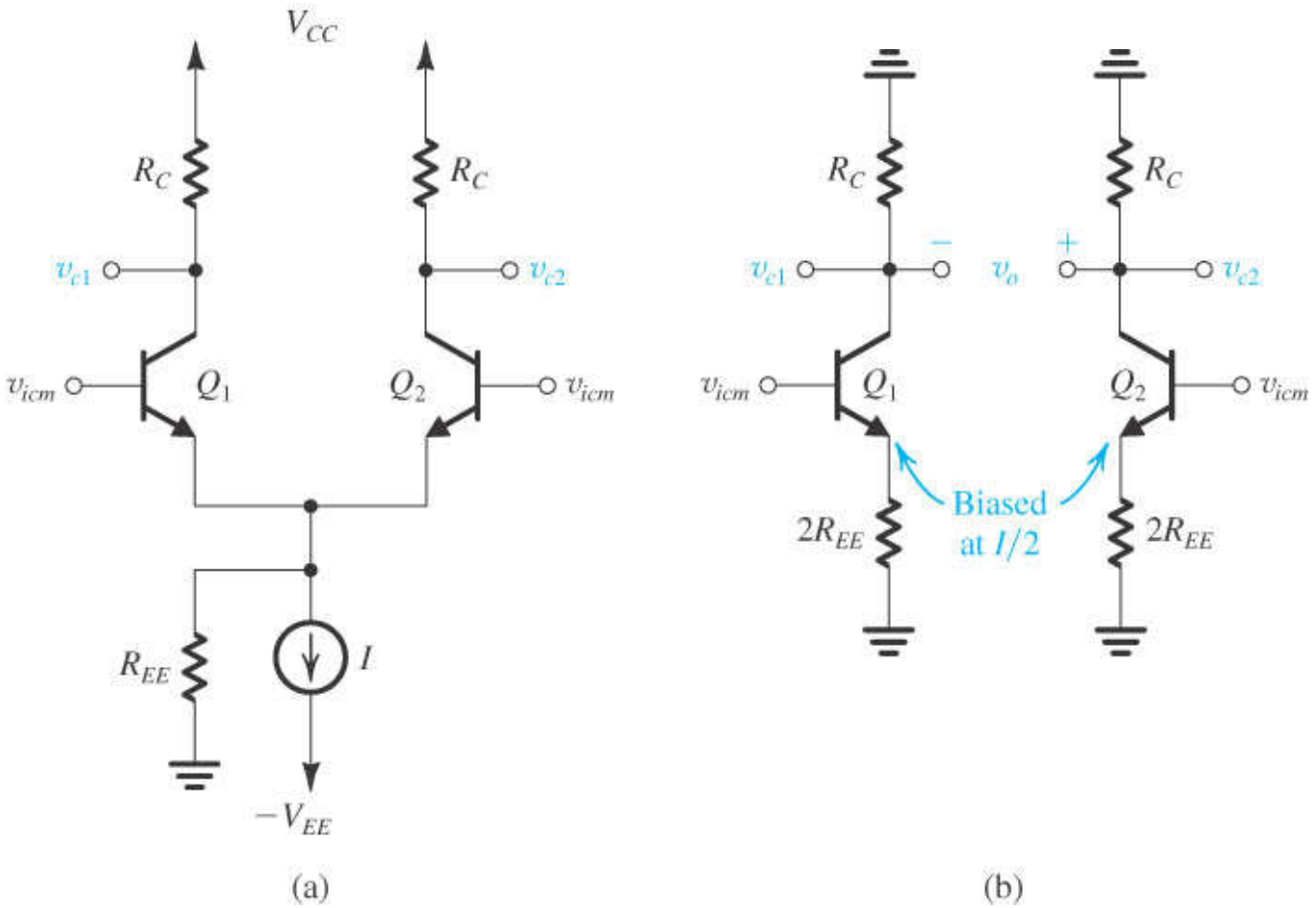

Figure 7.22 **(a)** The differential amplifier fed by a common-mode voltage signal v_{icm}. **(b)** Equivalent "half-circuits" for common-mode calculations.

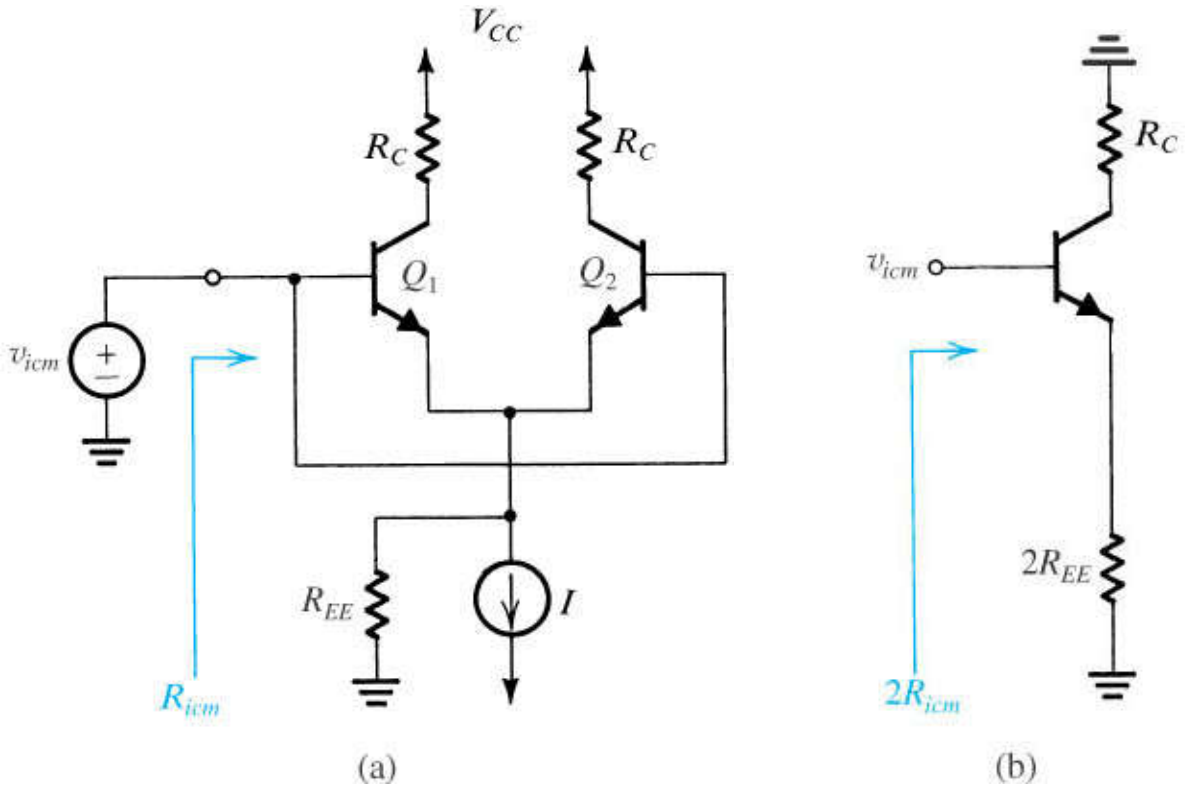

Figure 7.23 **(a)** Definition of the input common-mode resistance R_{icm}. (b) The equivalent common-mode half-circuit.

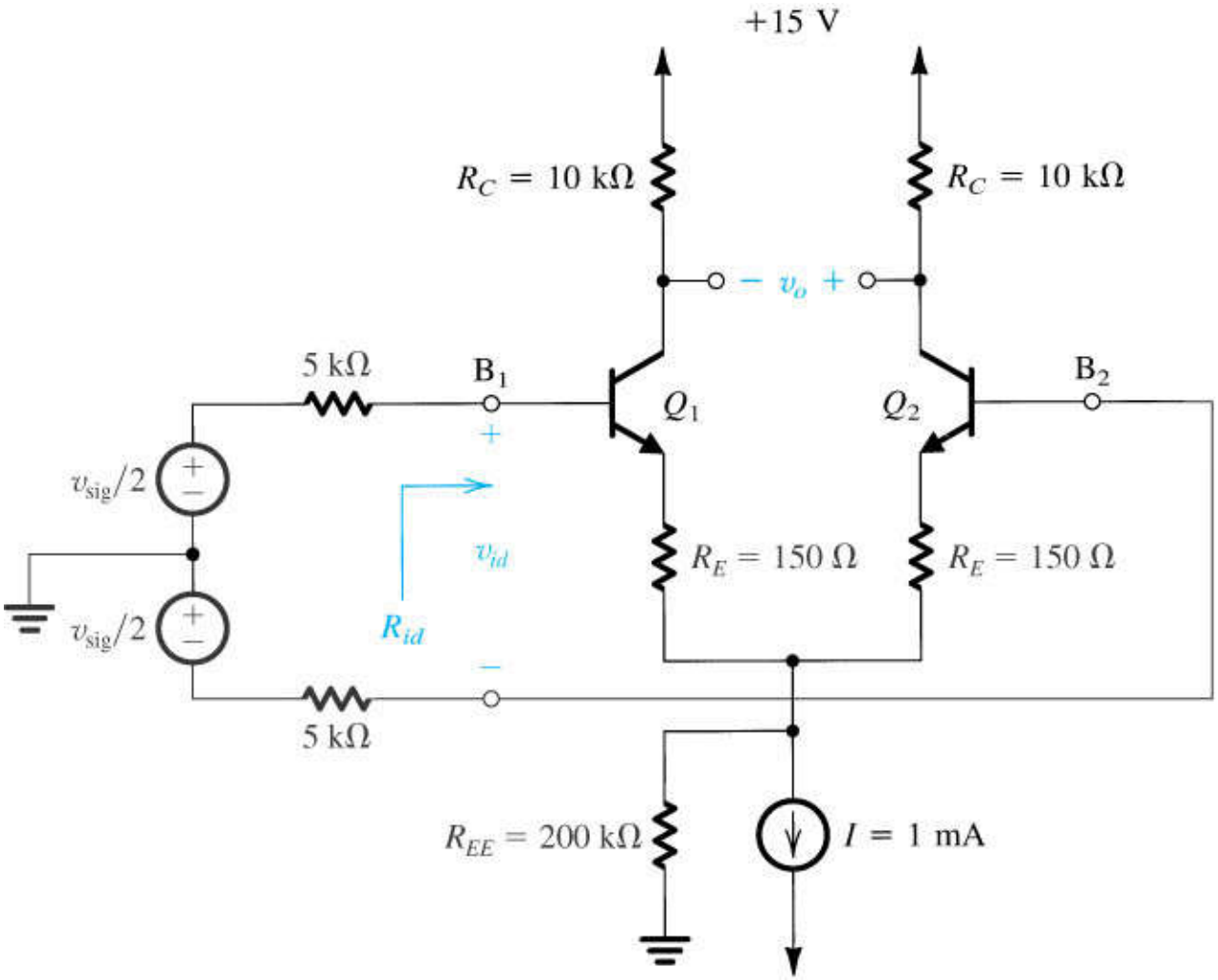

Figure 7.24 Circuit for Example 7.1.

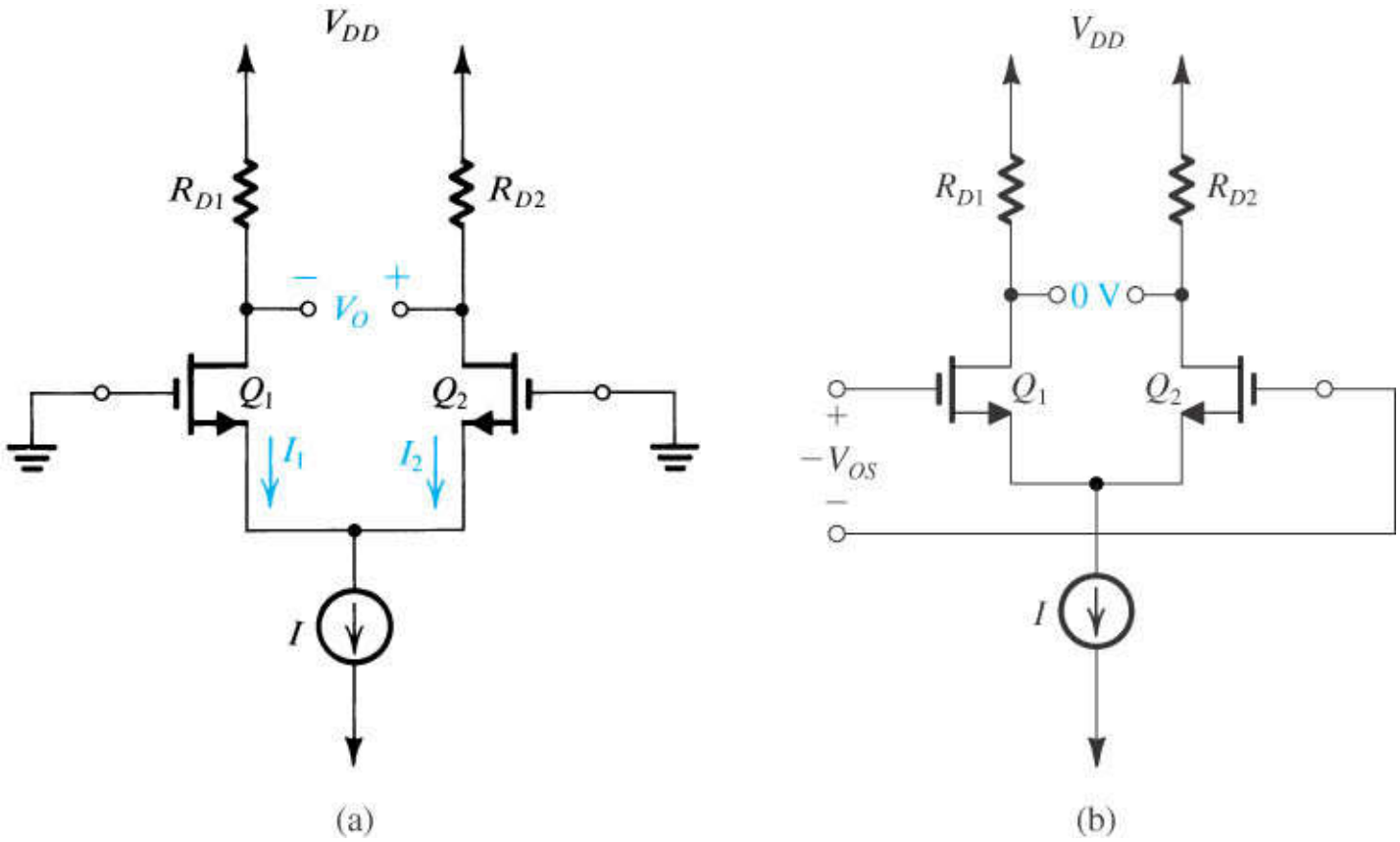

Figure 7.25 **(a)** The MOS differential pair with both inputs grounded. Owing to device and resistor mismatches, a finite dc output voltage V_O results. **(b)** Application of a voltage equal to the input offset voltage V_{OS} to the terminals with opposite polarity reduces V_O to zero.

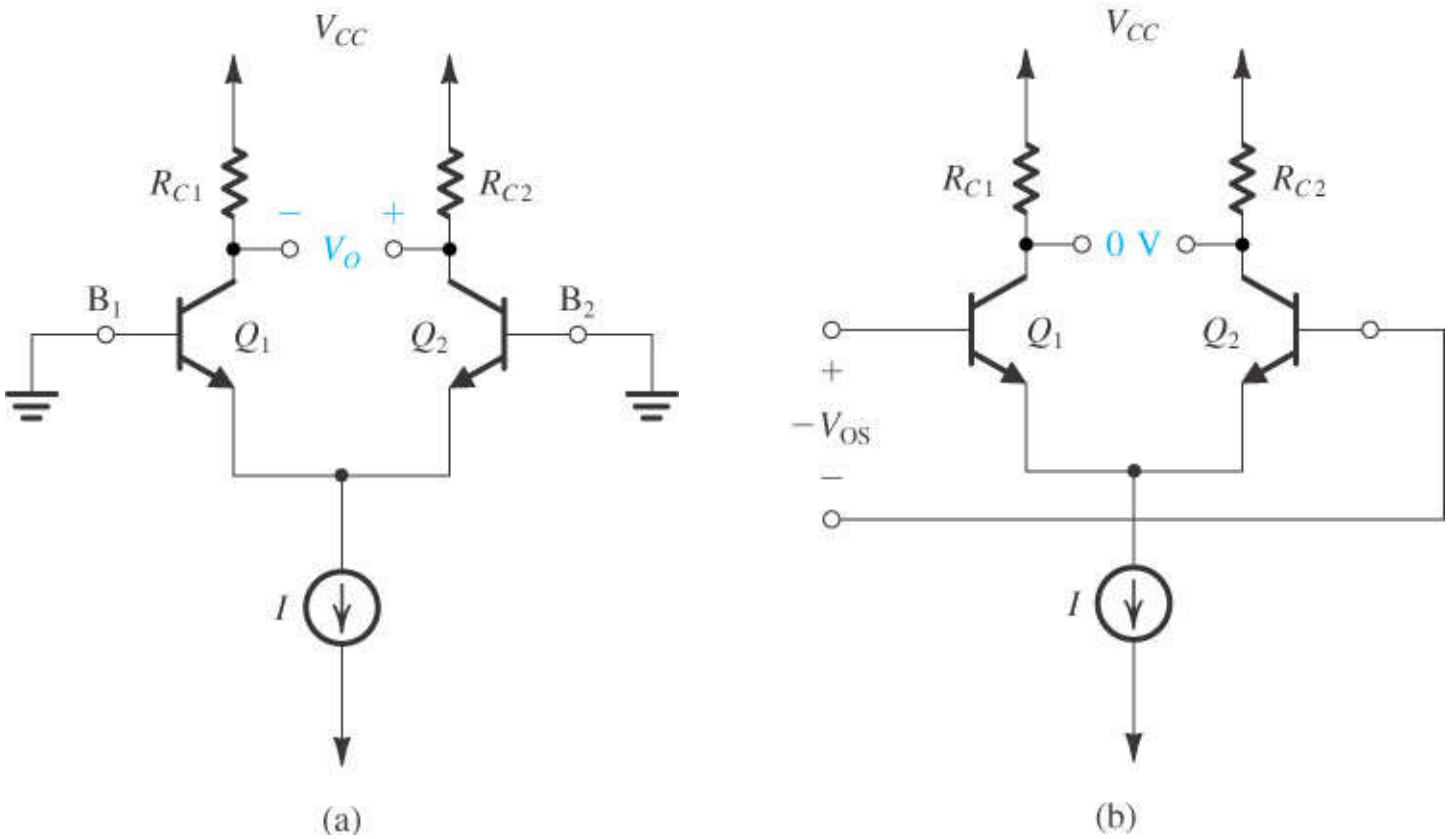

Figure 7.26 **(a)** The BJT differential pair with both inputs grounded. Device mismatches result in a finite dc output V_O. **(b)** Application of the input offset voltage V_{OS} ; V_O/A_d to the input terminals with opposite polarity reduces V_O to zero.

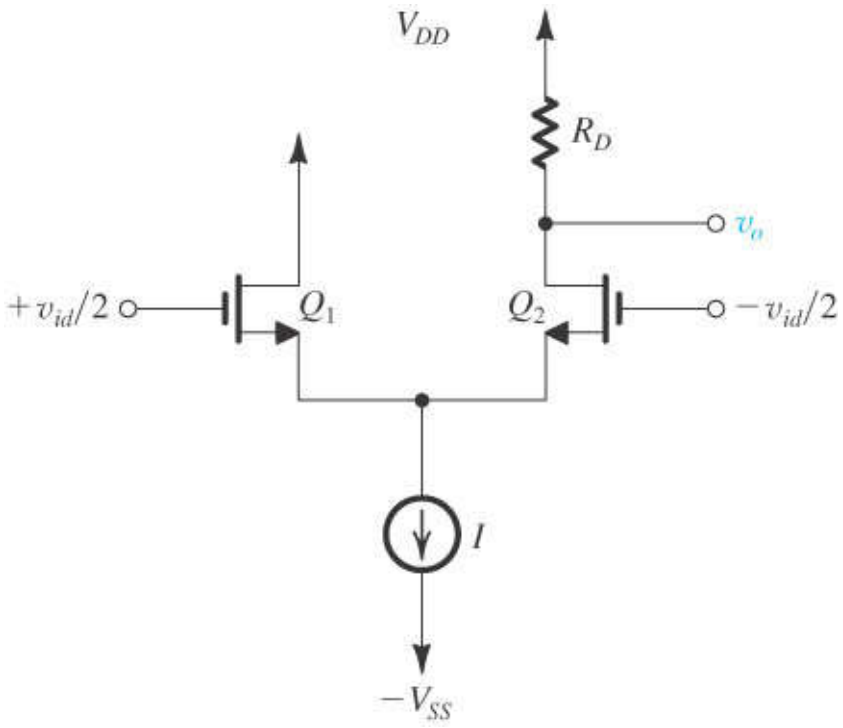

Figure 7.27 A simple but inefficient approach for differential to single-ended conversion.

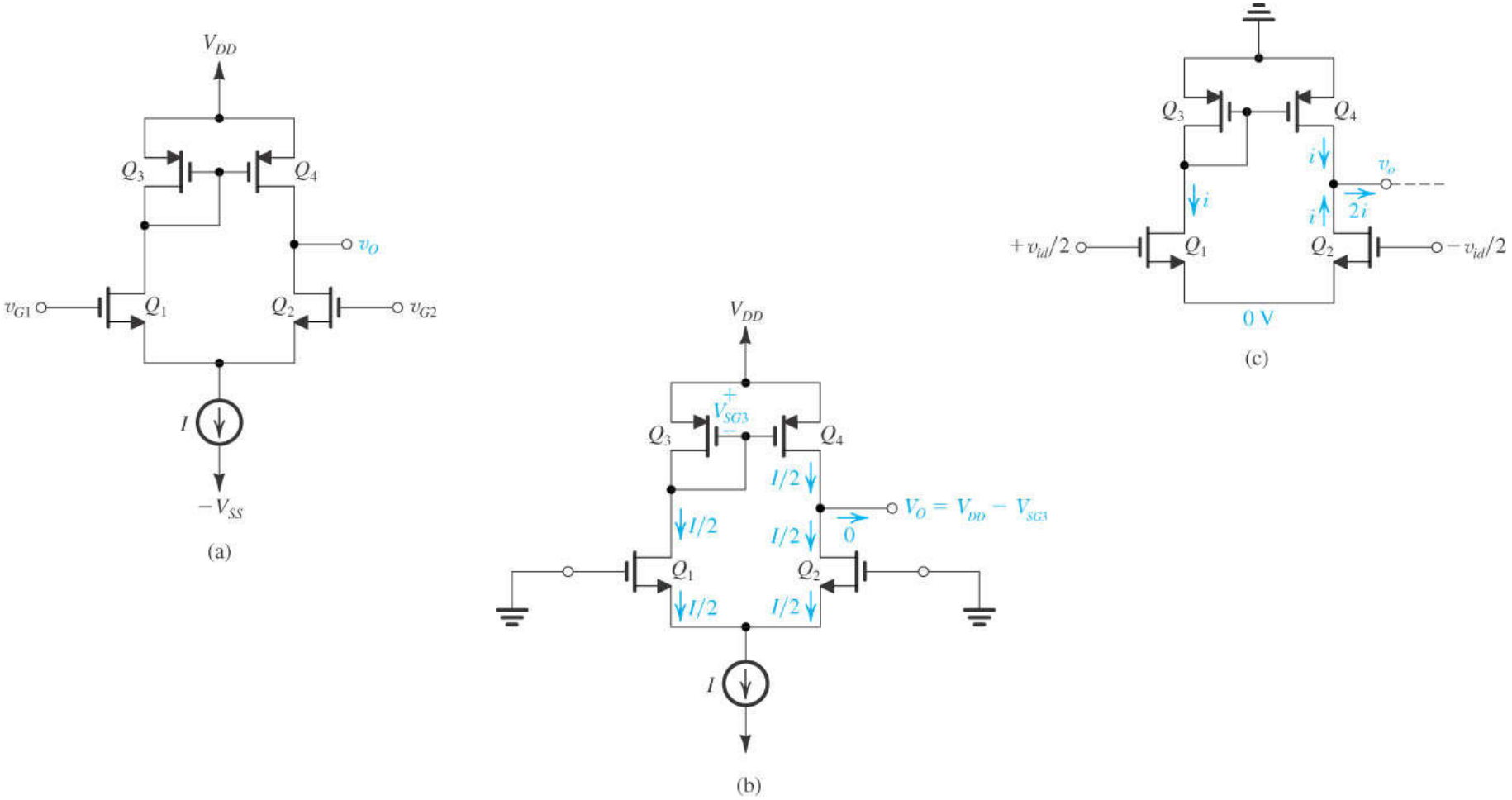

Figure 7.28 **(a)** The active-loaded MOS differential pair. **(b)** The circuit at equilibrium assuming perfect matching. **(c)** The circuit with a differential input signal applied, neglecting the r_o of all transistors.

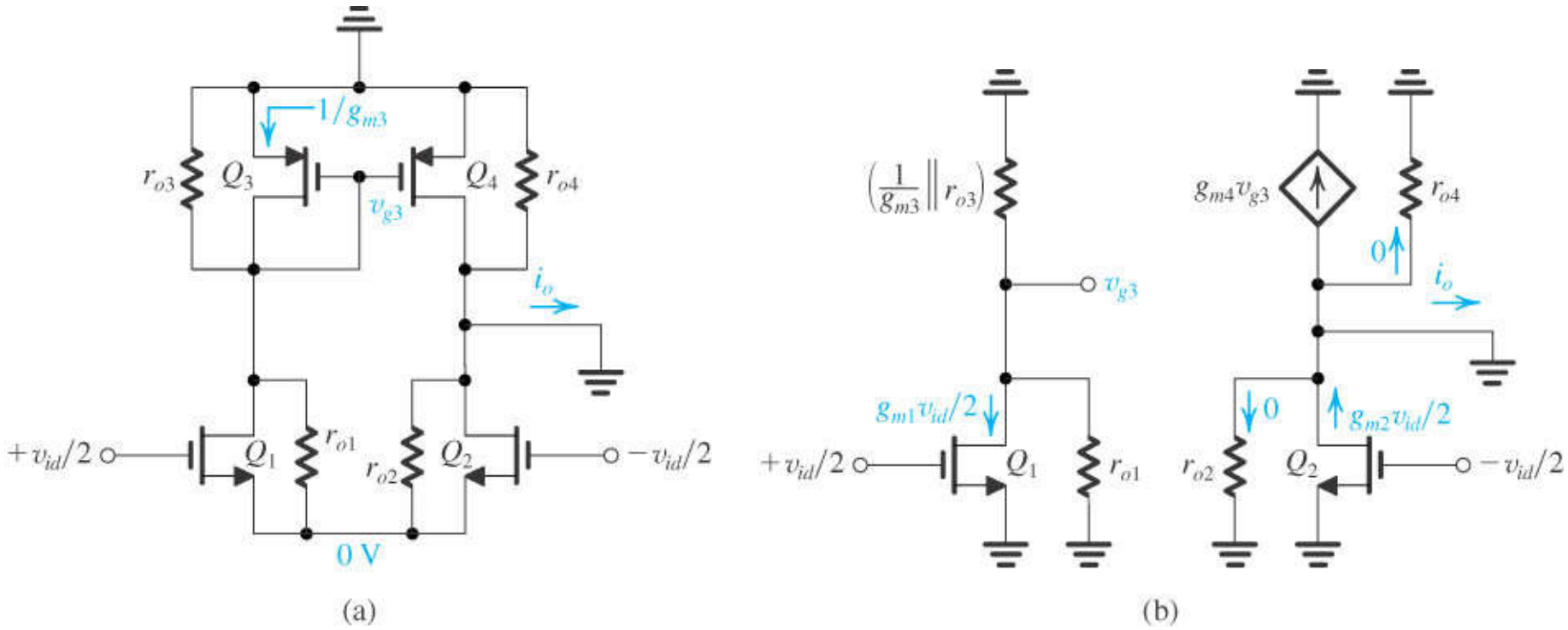

Figure 7.29 Determining the short-circuit transconductance G_m ; i_o/v_{id} of the active-loaded MOS differential pair.

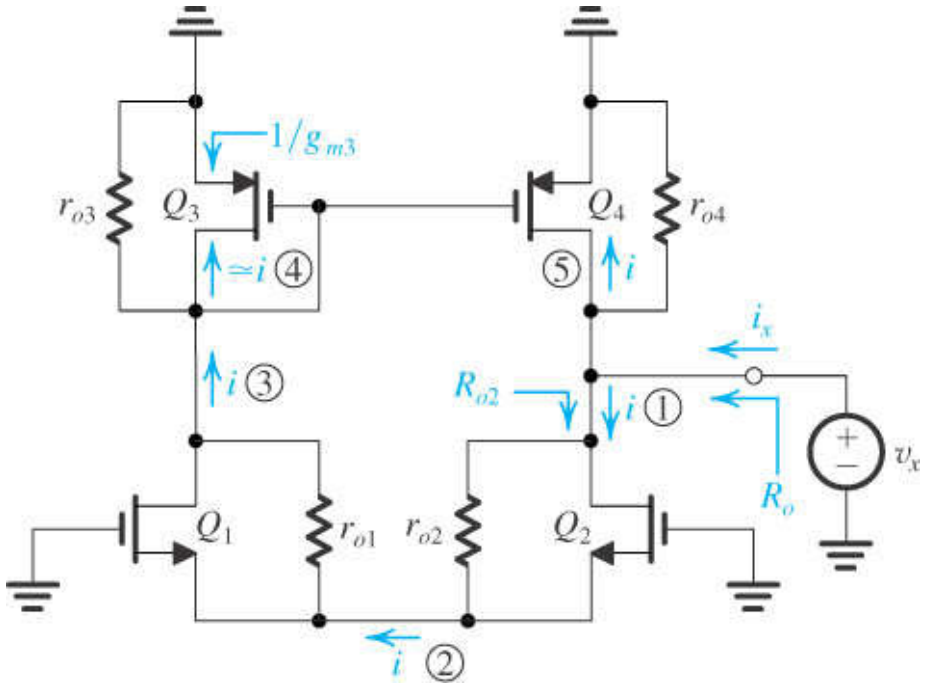

Figure 7.30 Circuit for determining R_o. The circled numbers indicate the order of the analysis steps.

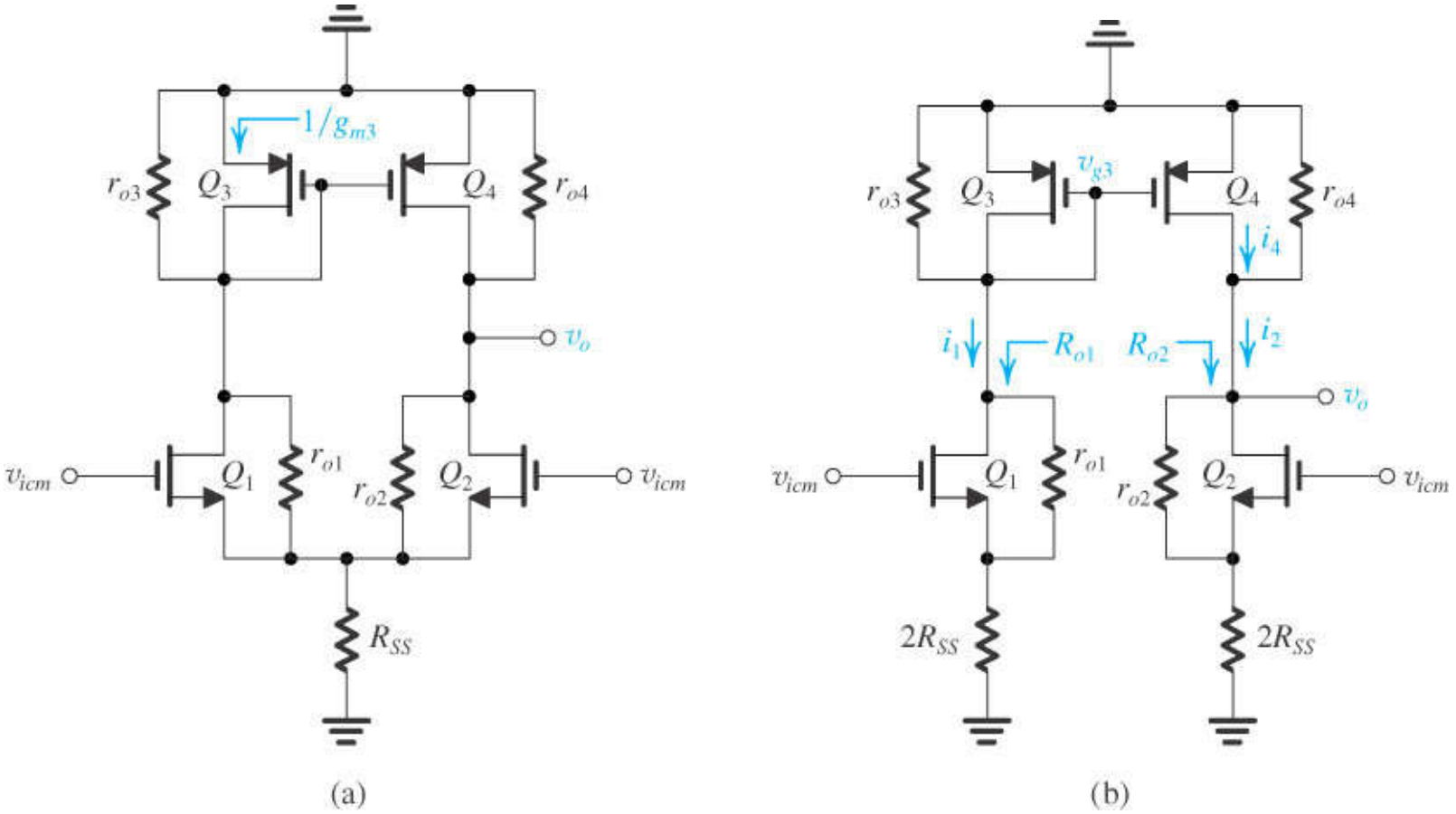

Figure 7.31 Analysis of the active-loaded MOS differential amplifier to determine its common-mode gain.

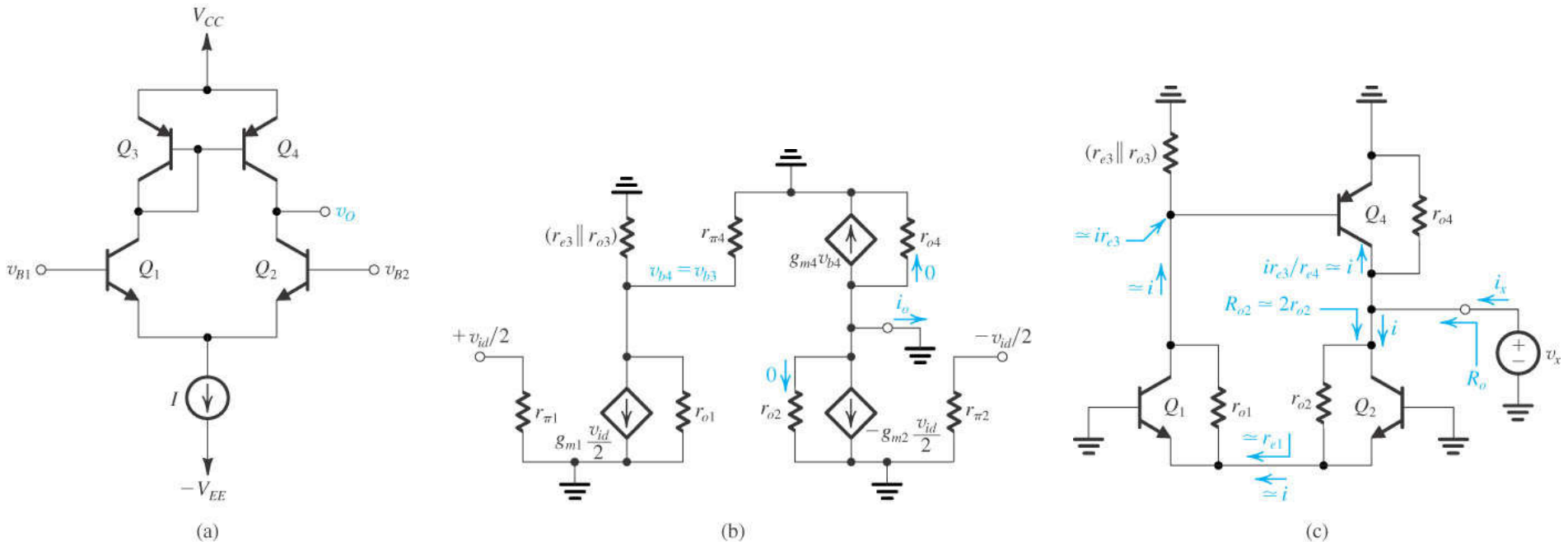

Figure 7.32 **(a)** Active-loaded bipolar differential pair. **(b)** Small-signal equivalent circuit for determining the transconductance G_m ; i_o/v_{id}. **(c)** Equivalent circuit for determining the output resistance R_o ; v_x/i_x.

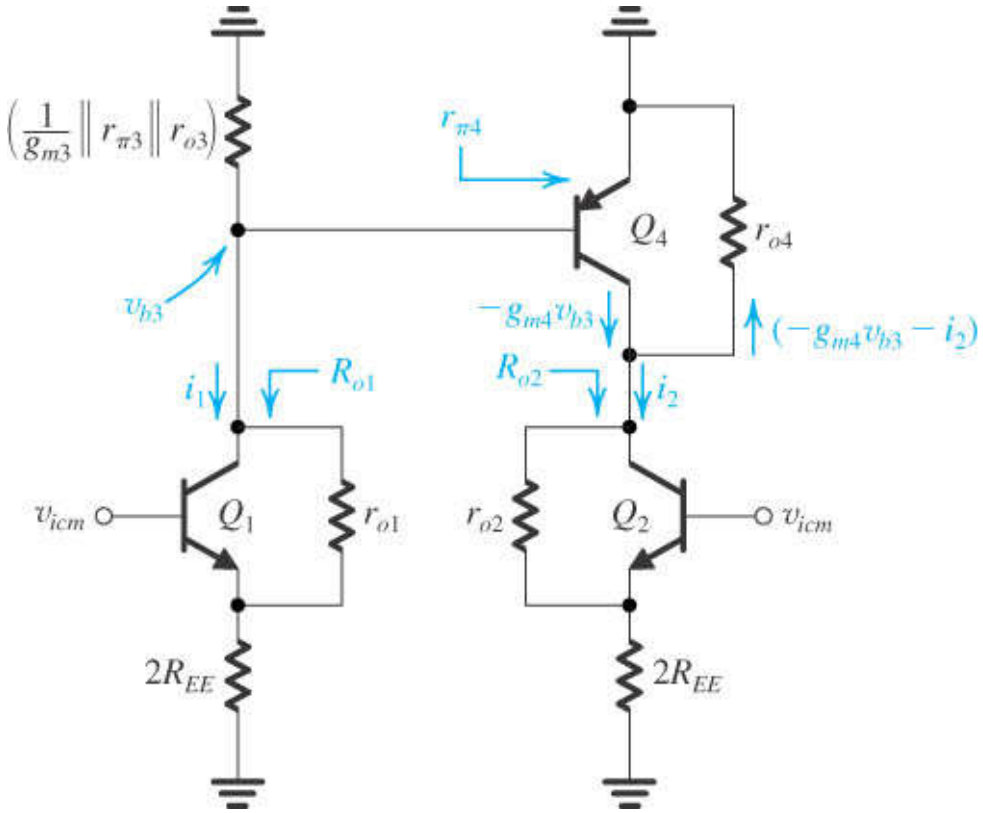

Figure 7.33 Analysis of the bipolar active-loaded differential amplifier to determine the common-mode gain.

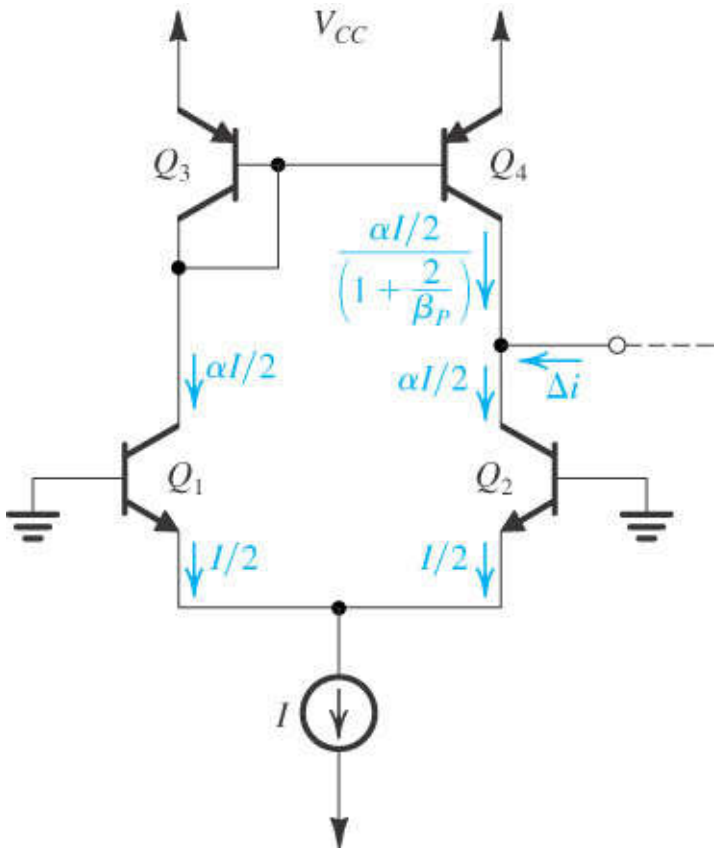

Figure 7.34 The active-loaded BJT differential pair suffers from a systematic input offset voltage resulting from the error in the current-transfer ratio of the current mirror.

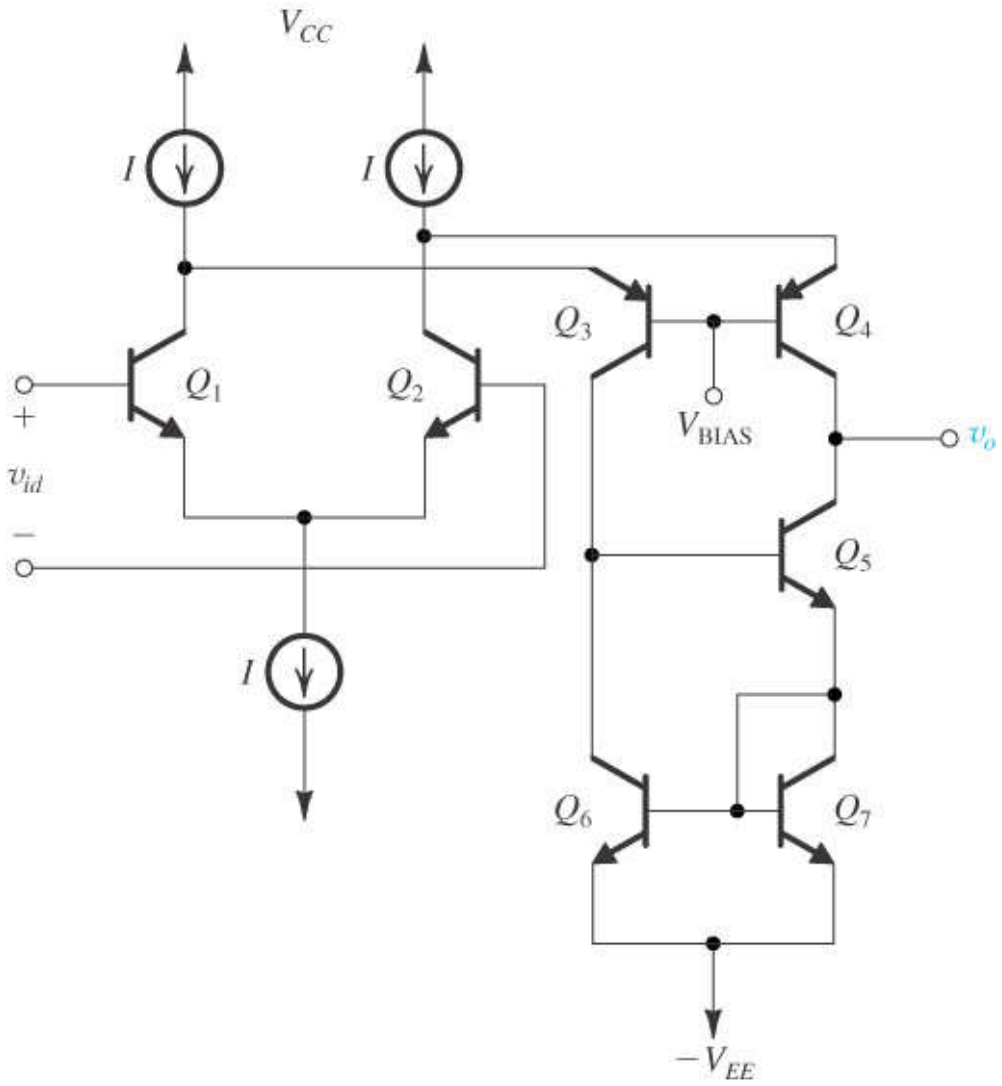

Figure 7.35 An active-loaded bipolar differential amplifier employing a folded cascode stage (Q_3 and Q_4) and a Wilson current mirror load (Q_5, Q_6, and Q_7).

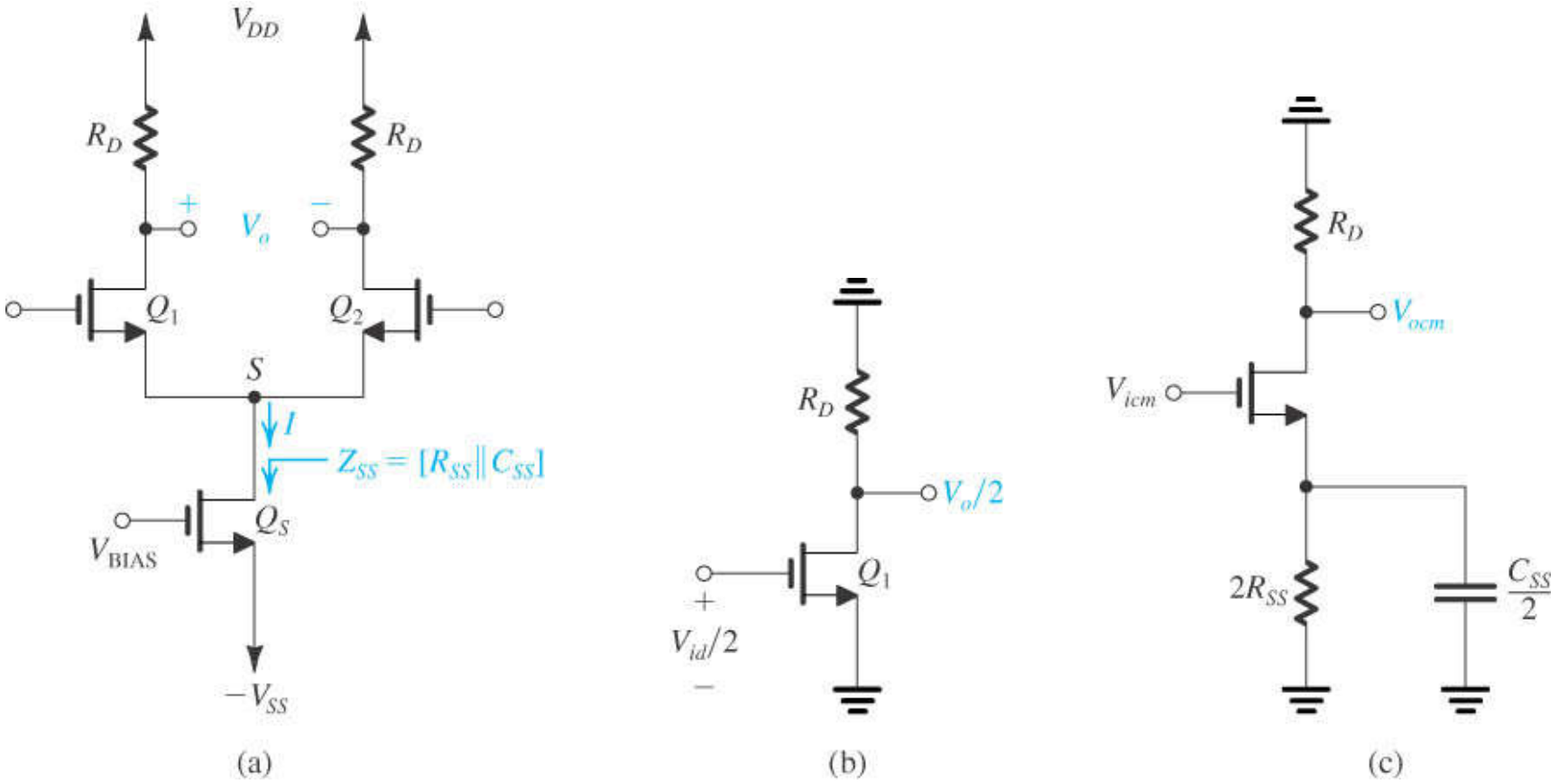

Figure 7.36 **(a)** A resistively loaded MOS differential pair with the transistor supplying the bias current explicitly shown. It is assumed that the total impedance between node S and ground, Z_{SS}, consists of a resistance R_{SS} in parallel with a capacitance C_{SS}. **(b)** Differential half-circuit. **(c)** Common-mode half-circuit.

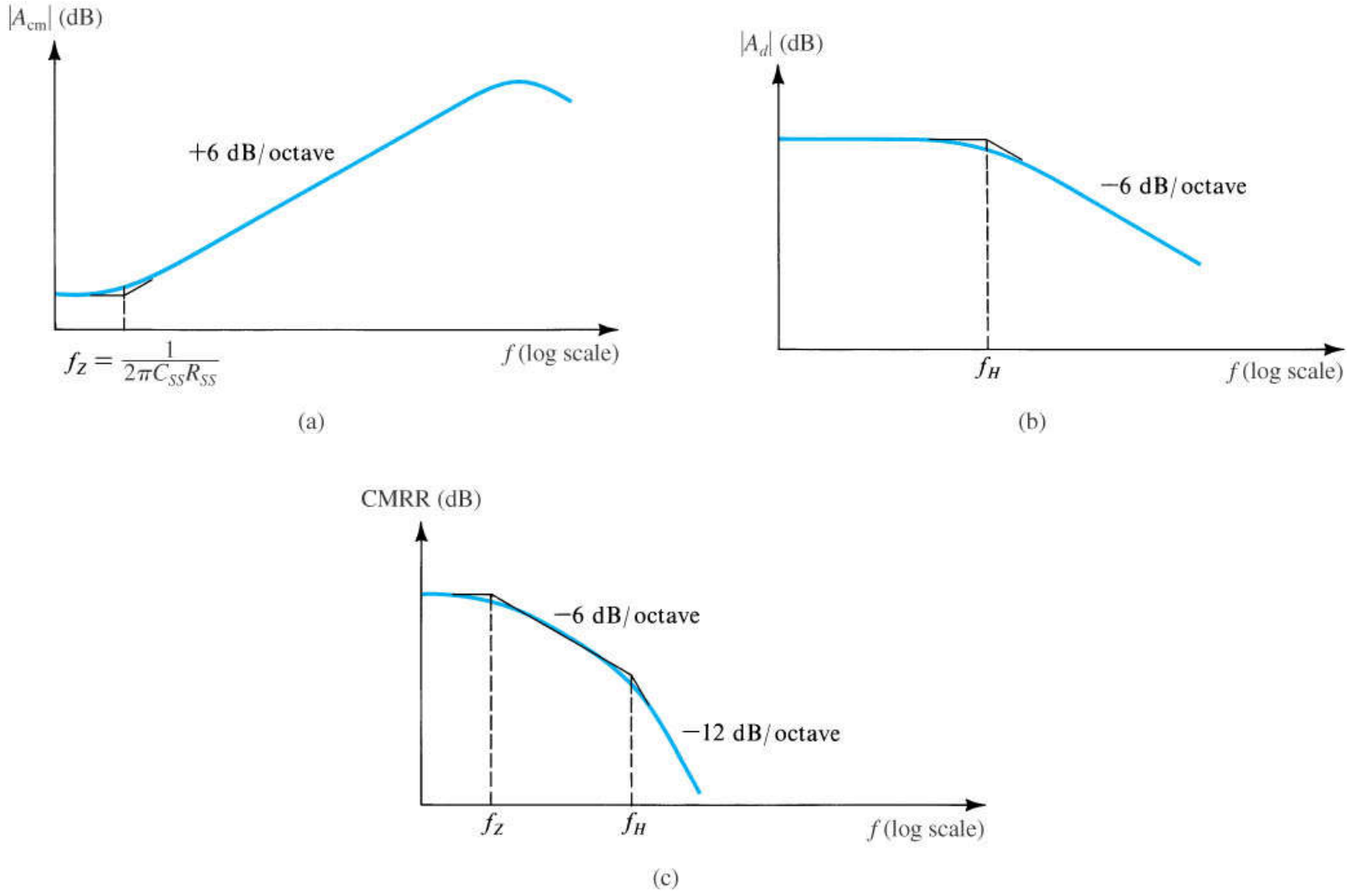

Figure 7.37 Variation of **(a)** common-mode gain, **(b)** differential gain, and **(c)** common-mode rejection ratio with frequency.

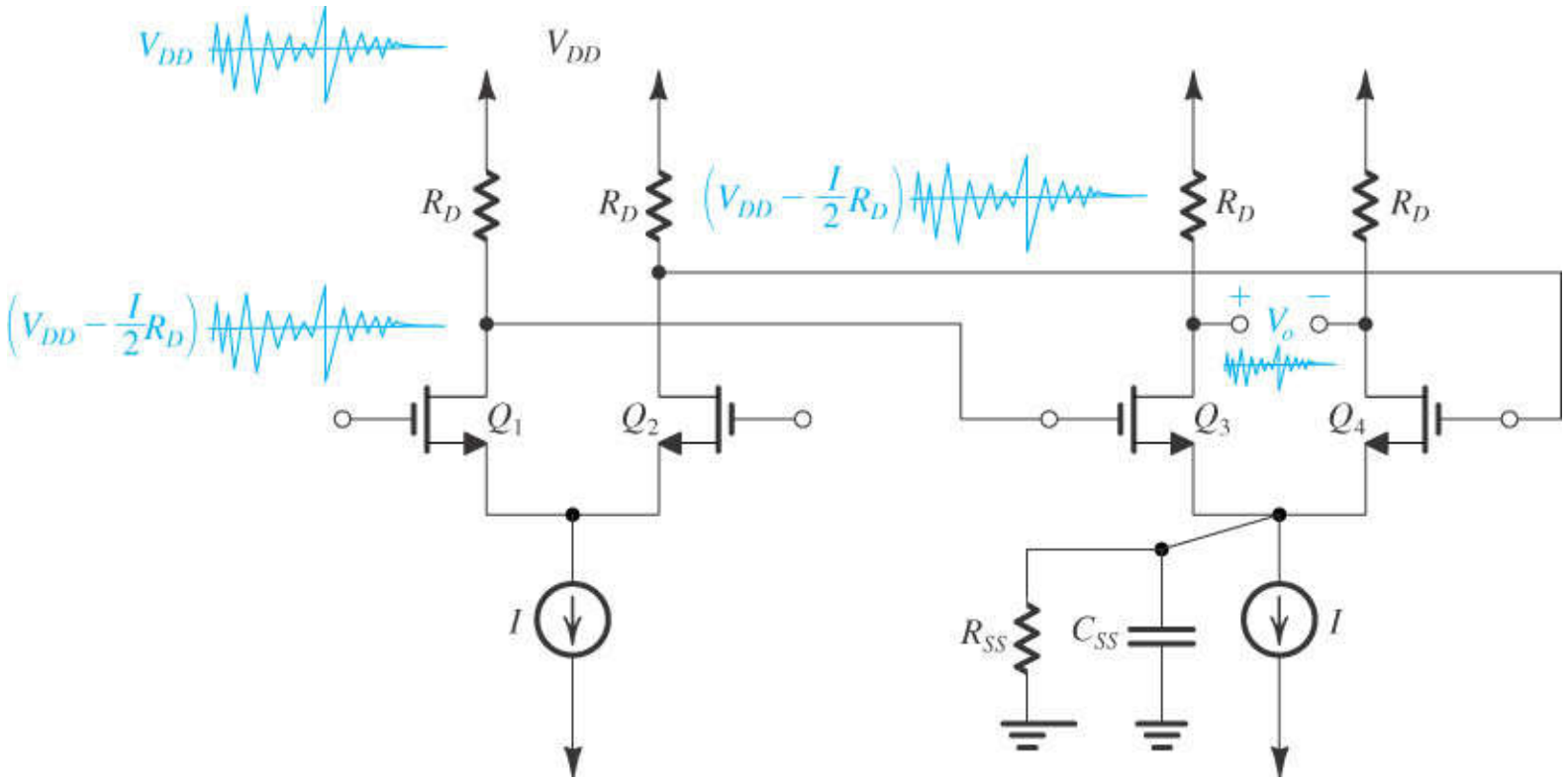

Figure 7.38 The second stage in a differential amplifier is relied on to suppress high-frequency noise injected by the power supply of the first stage, and therefore must maintain a high CMRR at higher frequencies.

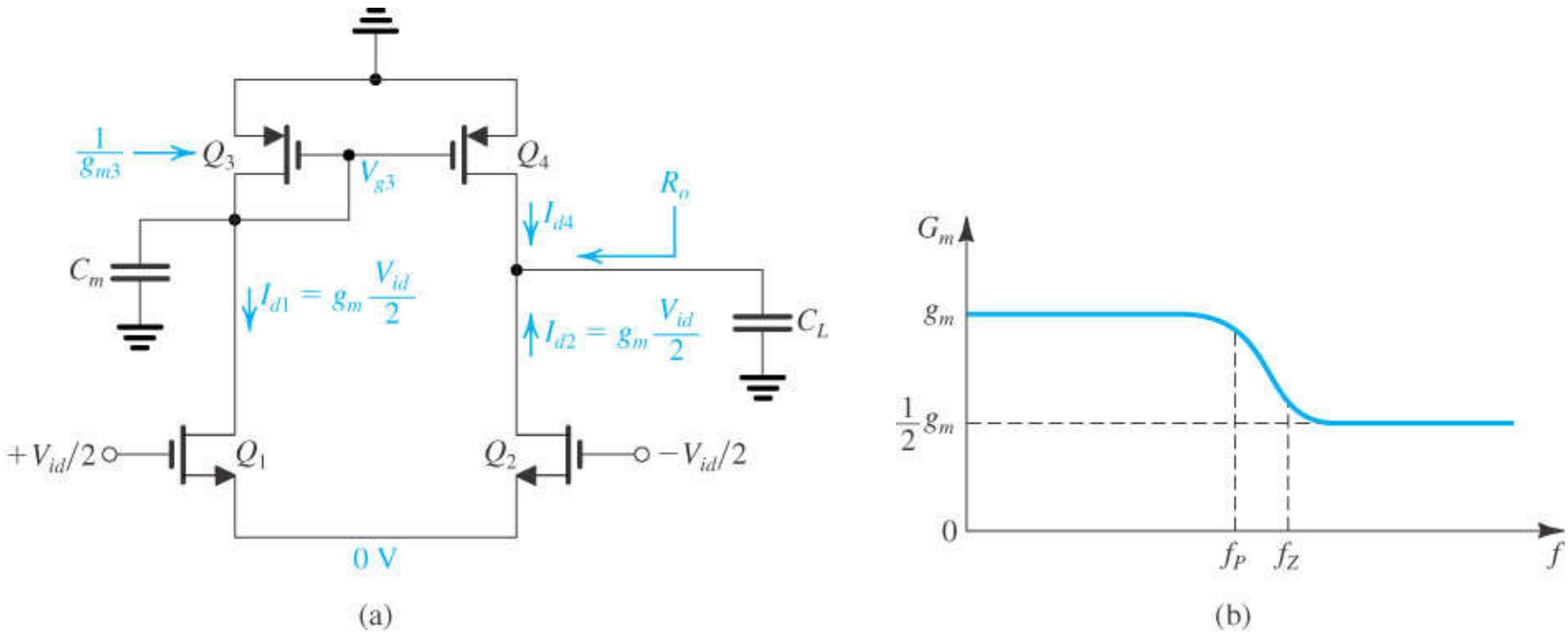

Figure 7.39 **(a)** Frequency-response analysis of the active-loaded MOS differential amplifier. **(b)** The overall transconductance G_m as a function of frequency.

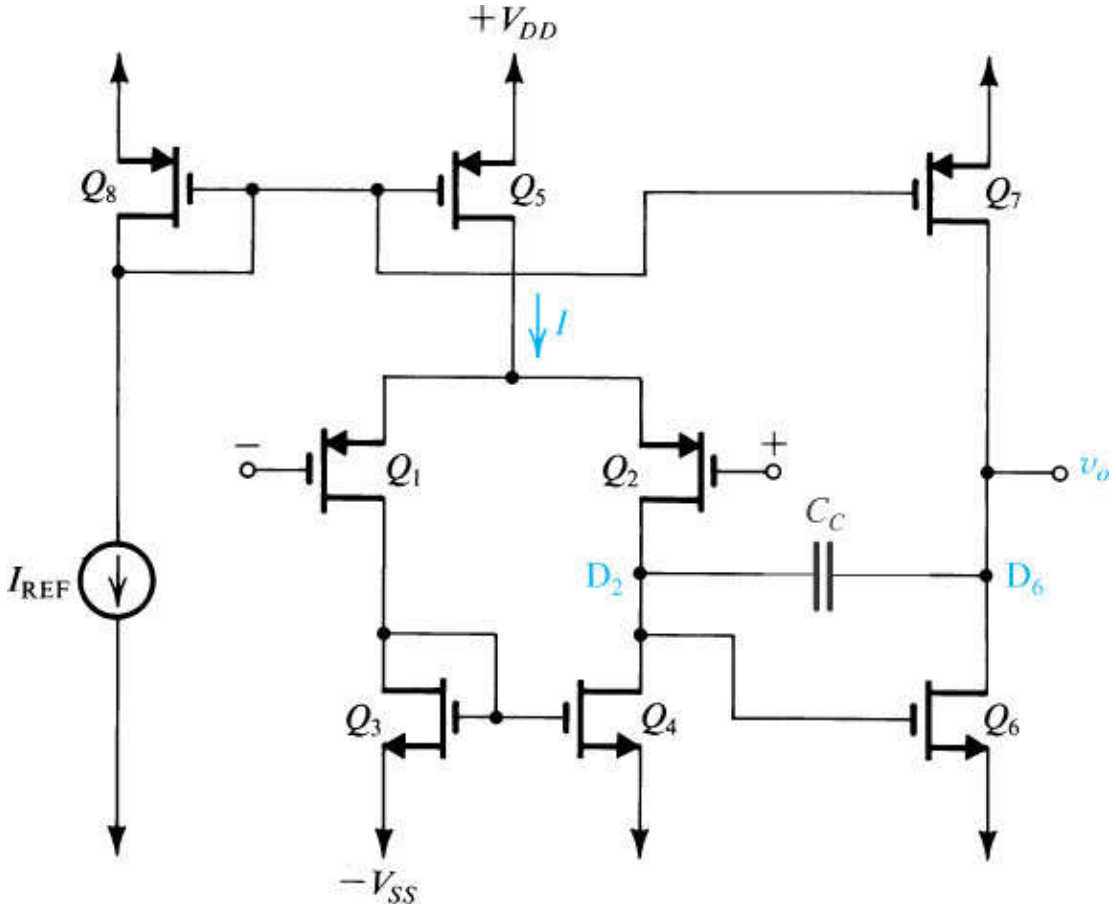

Figure 7.40 Two-stage CMOS op-amp configuration.

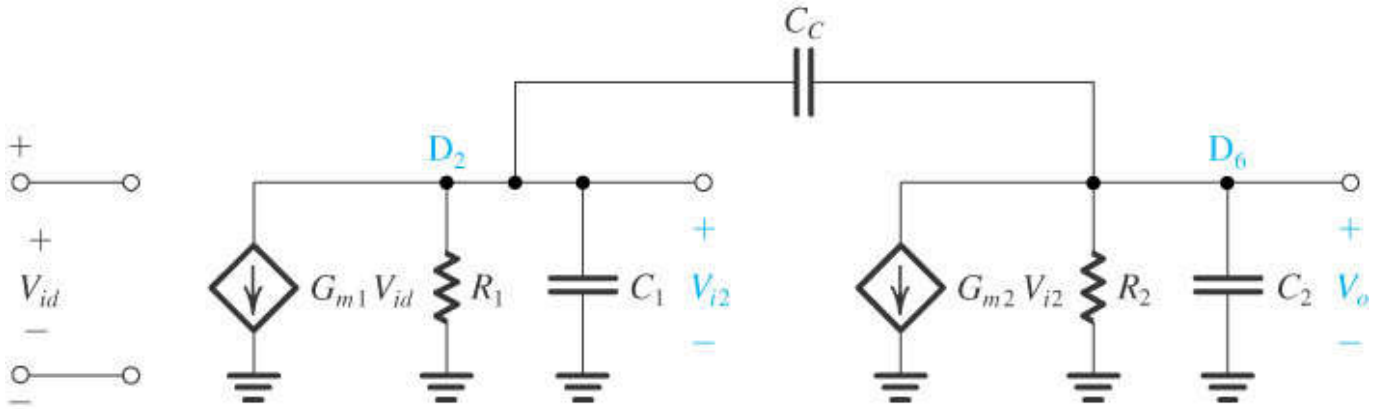

Figure 7.41 Equivalent circuit of the op amp in Fig. 7.40.

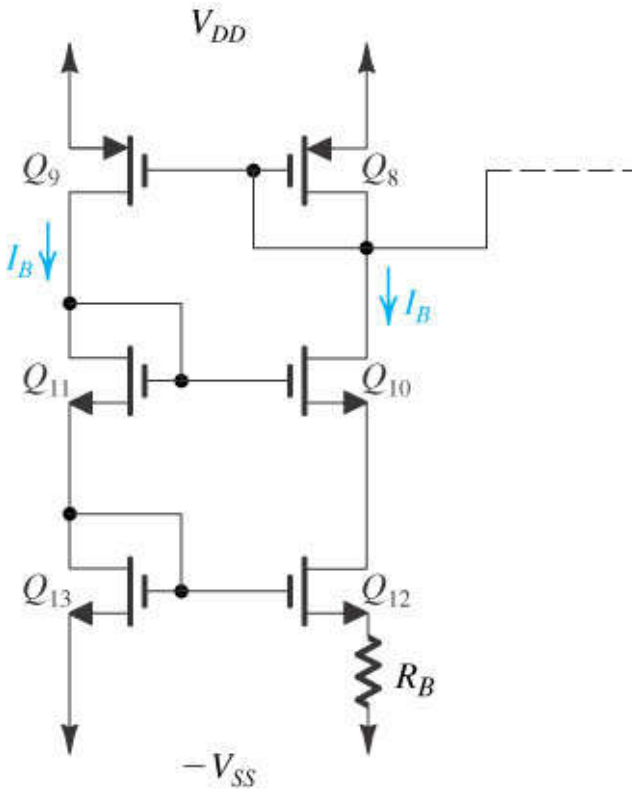

Figure 7.42 Bias circuit for the CMOS op amp.

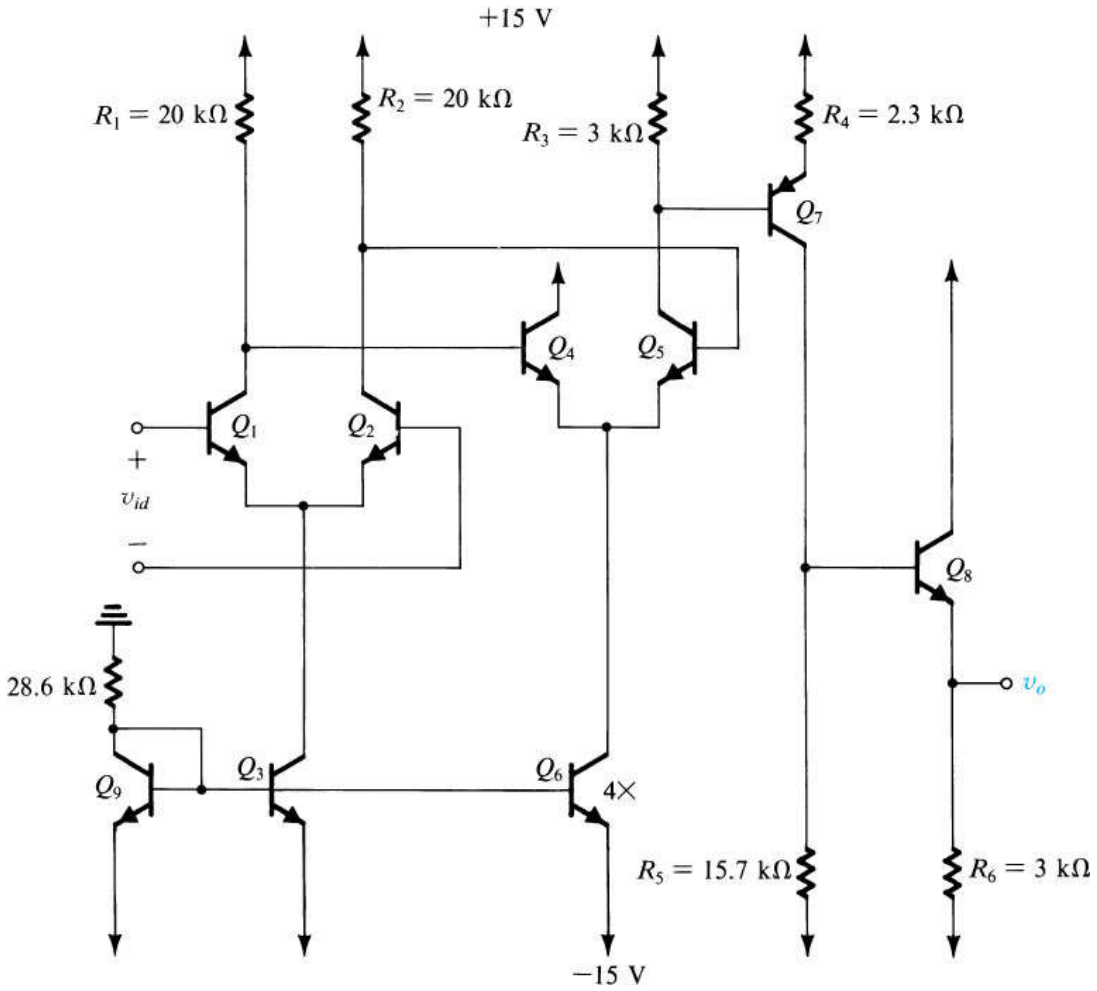

Figure 7.43 A four-stage bipolar op amp.

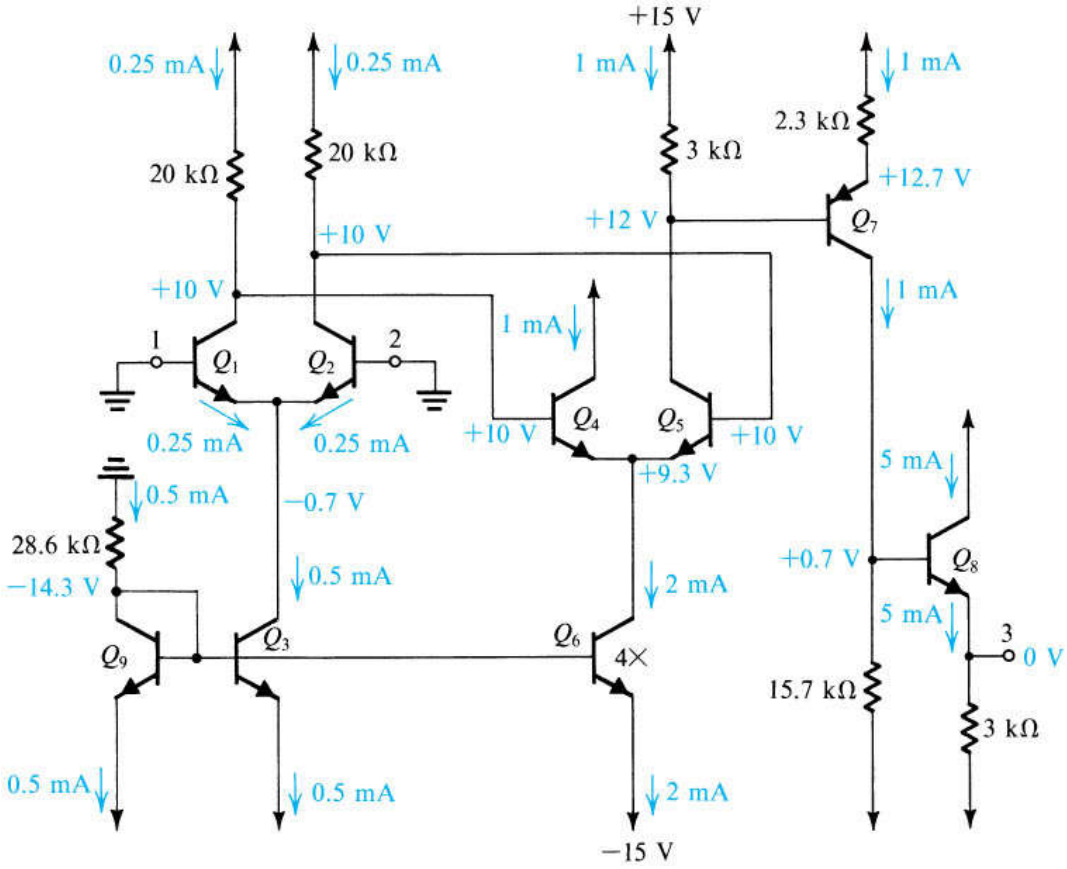

Figure 7.44 Circuit for Example 7.4.

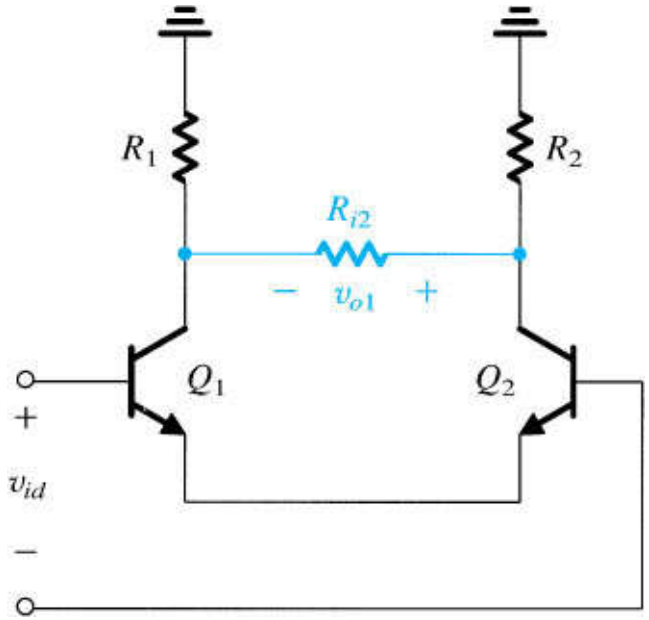

Figure 7.45 Equivalent circuit for calculating the gain of the input stage of the amplifier in Fig. 7.43.

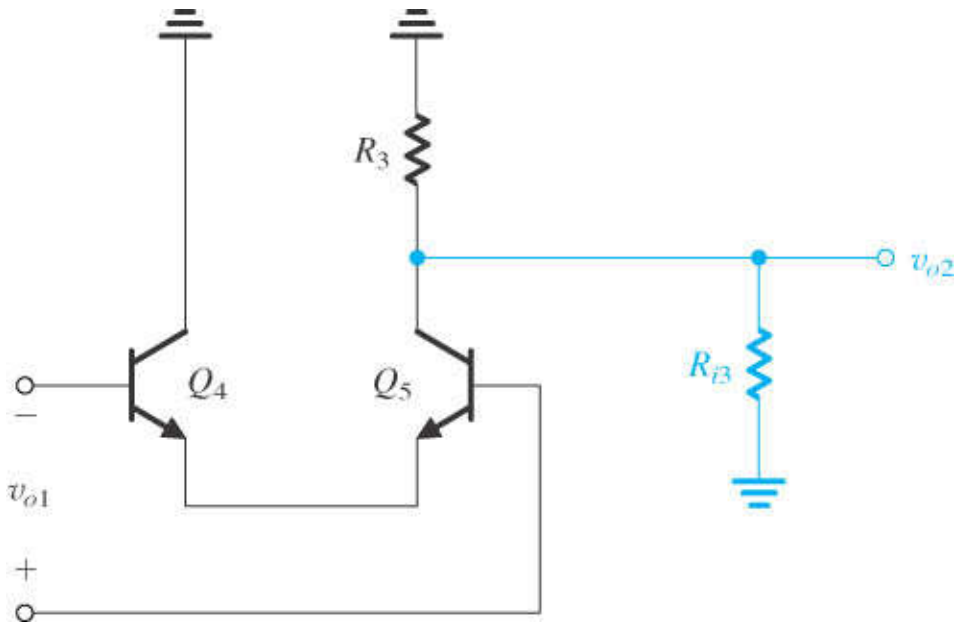

Figure 7.46 Equivalent circuit for calculating the gain of the second stage of the amplifier in Fig. 7.43.

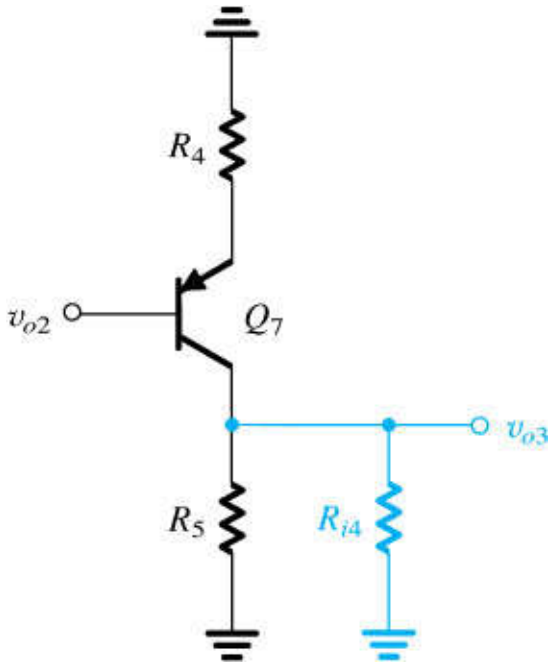

Figure 7.47 Equivalent circuit for evaluating the gain of the third stage in the amplifier circuit of Fig. 7.43.

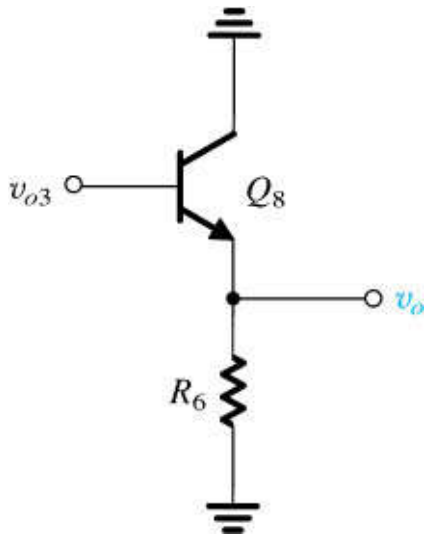

Figure 7.48 Equivalent circuit of the output stage of the amplifier circuit of Fig. 7.43.

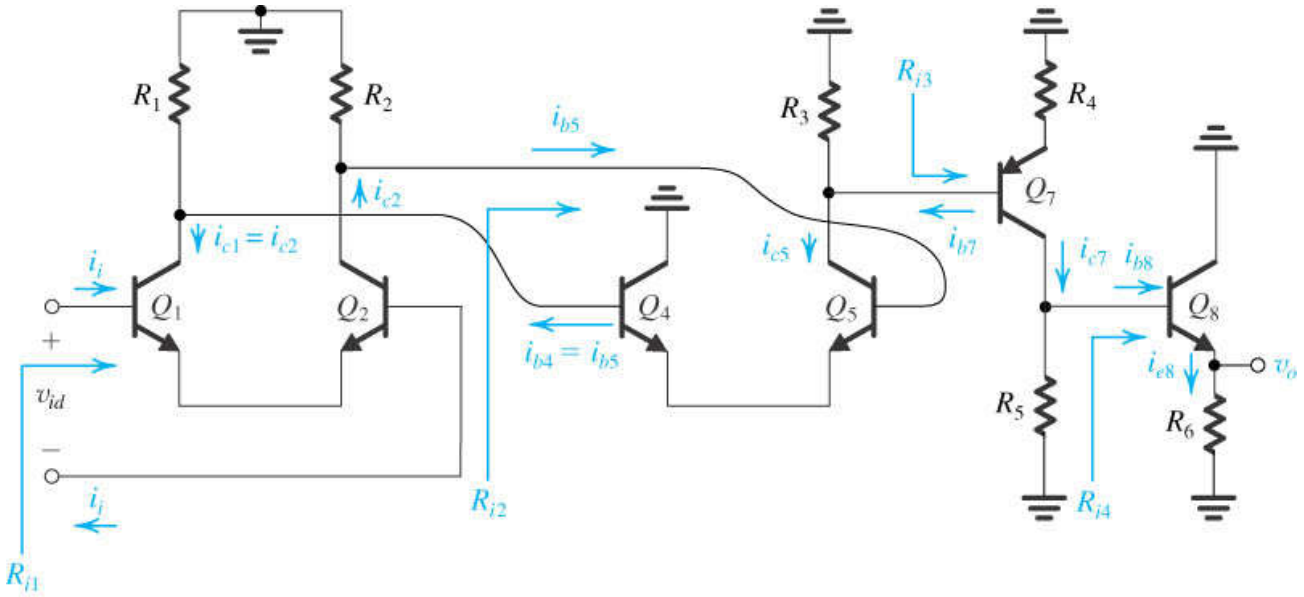

Figure 7.49 The circuit of the multistage amplifier of Fig. 7.43 prepared for small-signal analysis. Indicated are the signal currents throughout the amplifier and the input resistances of the four stages.

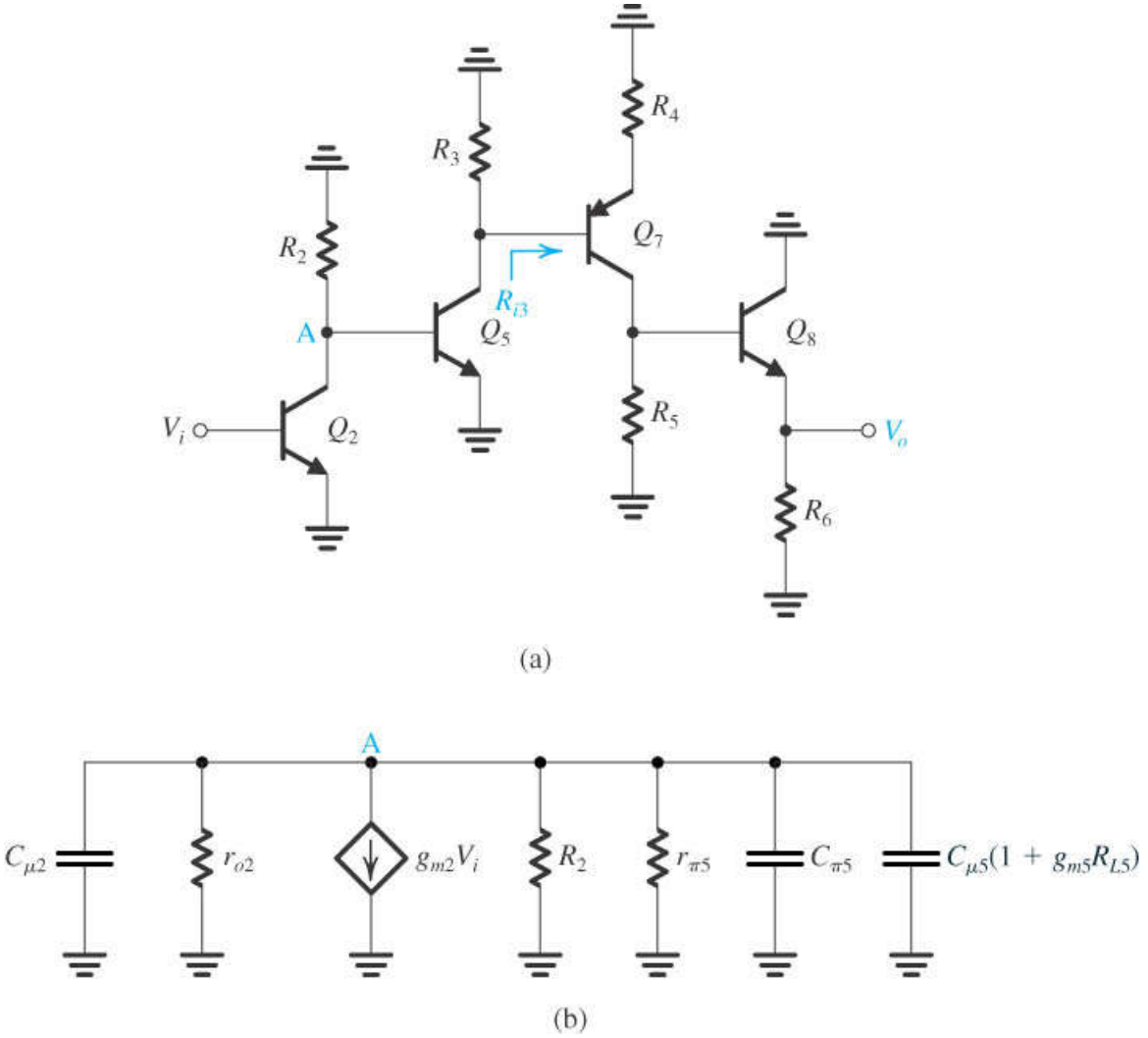

Figure 7.50 **(a)** Approximate equivalent circuit for determining the high-frequency response of the op amp of Fig. 7.43. **(b)** Equivalent circuit of the interface between the output of Q_2 and the input Q_5.

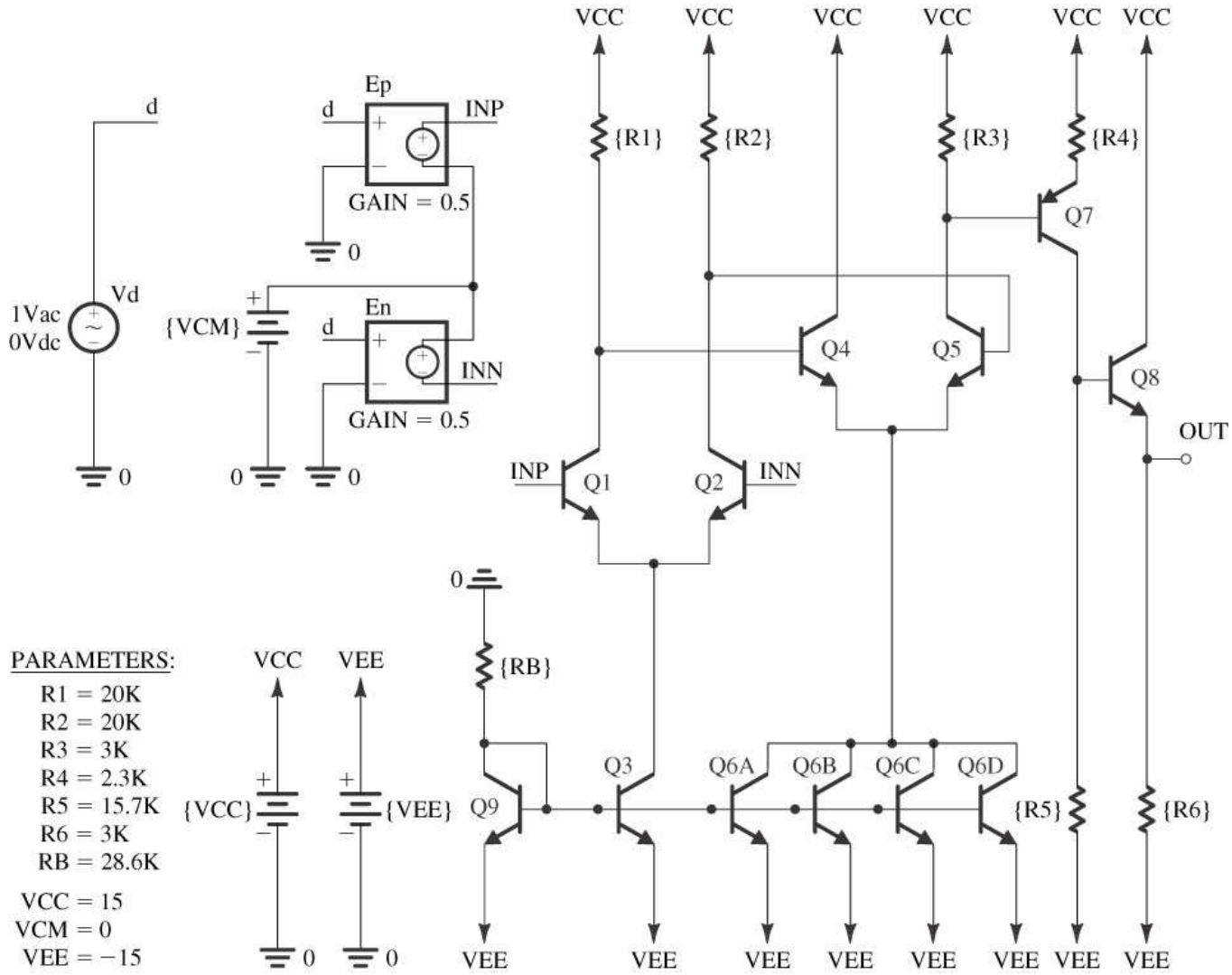

Figure 7.51 Capture schematic of the op-amp circuit in Fig. 7.51.

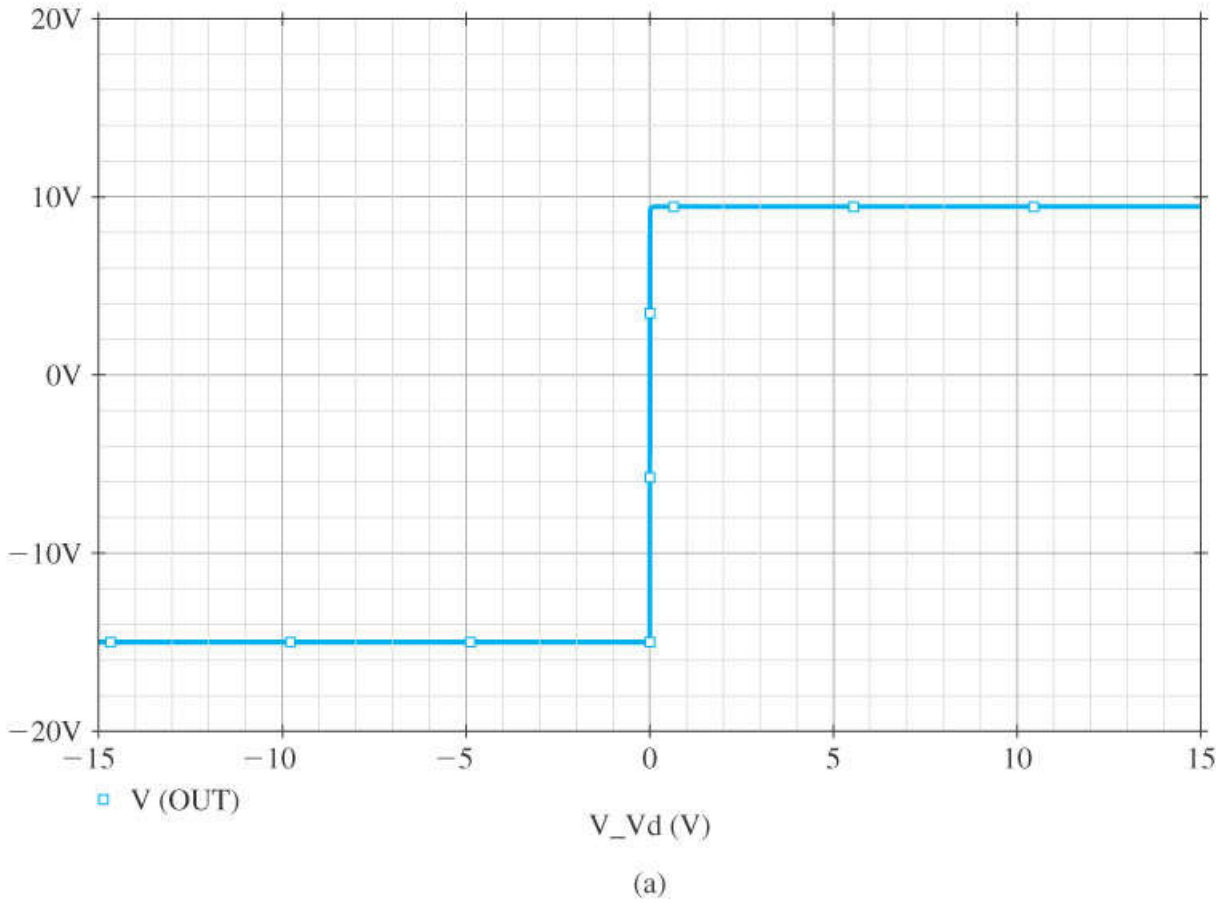

Figure 7.52 (a) The large-signal differential transfer characteristic of the op-amp circuit in Fig. 7.51. The common-mode input voltage VCM is set to 0 V.

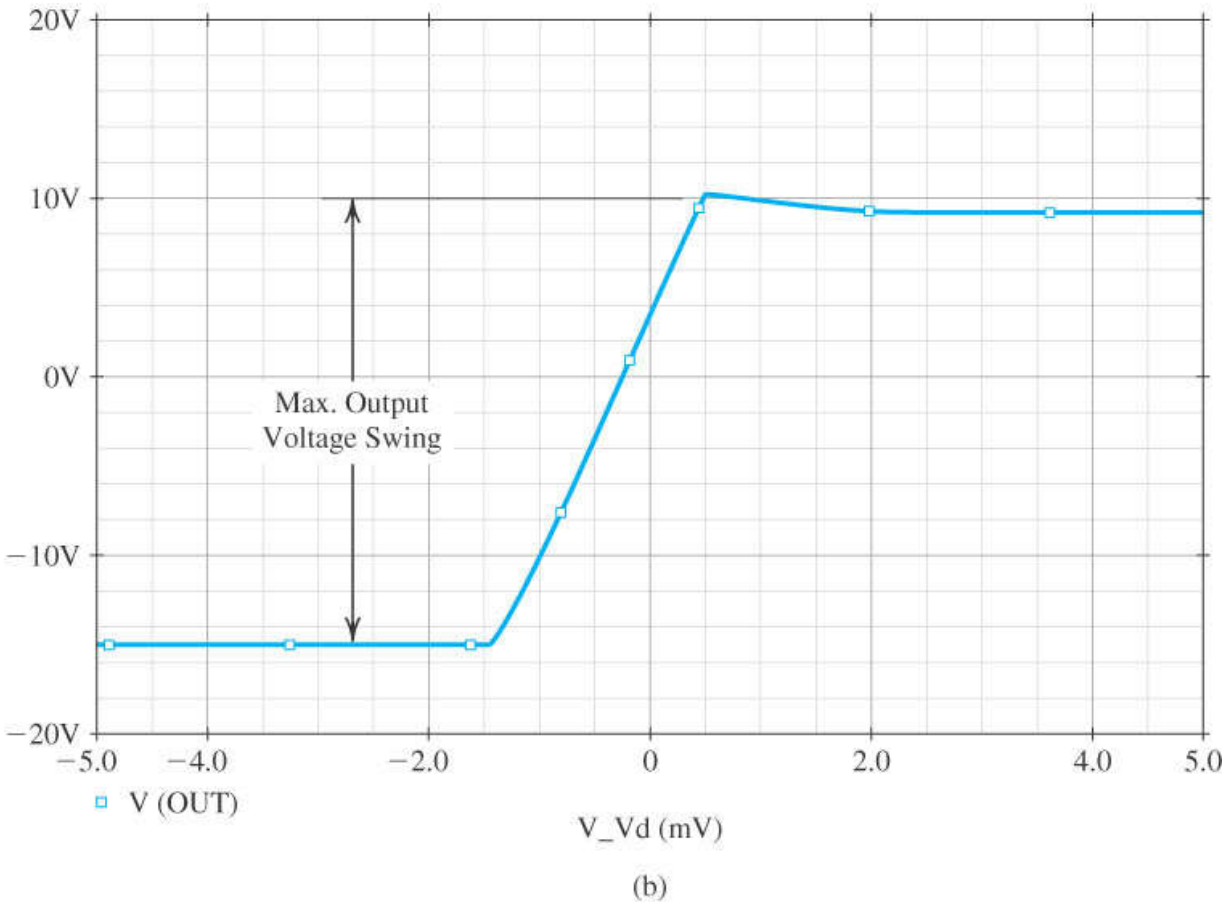

Figure 7.52 *(Continued)* **(b)** An expanded view of the transfer characteristic around the high-gain region.

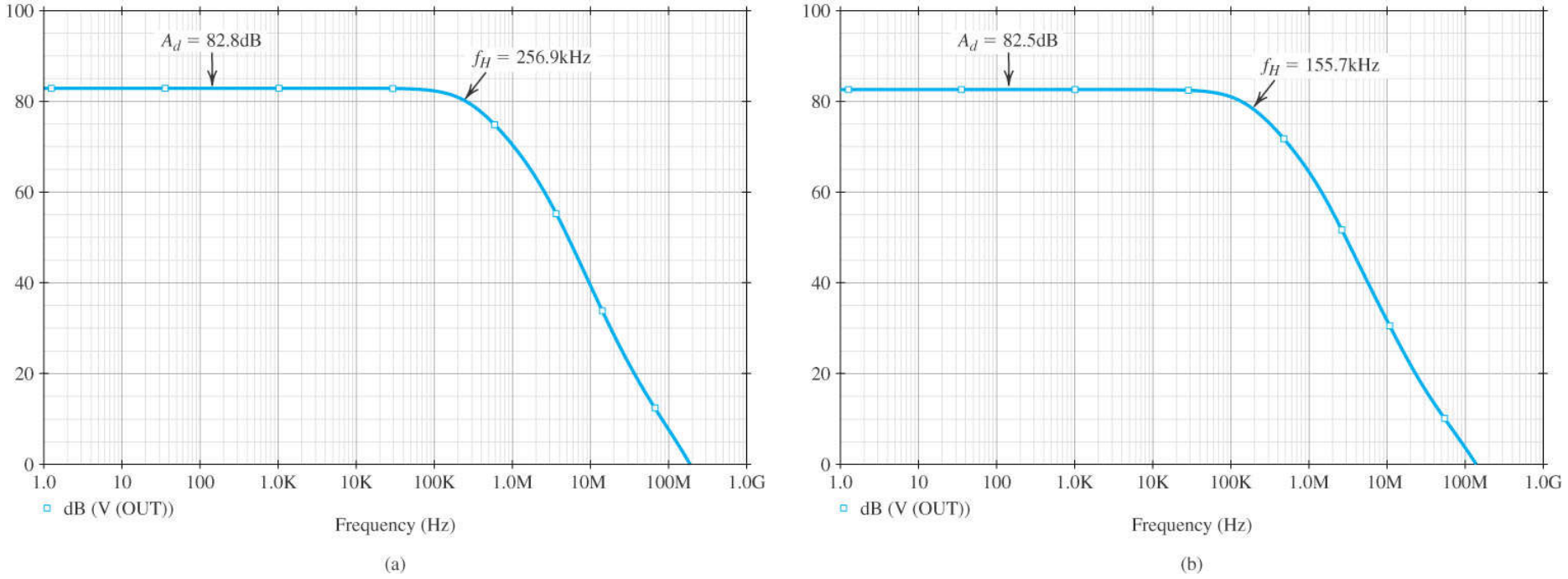

Figure 7.53 Frequency response of **(a)** the op-amp circuit in Fig. 7.51 and **(b)** the op-amp circuit in Fig. 7.51 but with a resistor $R'_3 = R_3$ inserted in the collector of Q_4 to make the op-amp circuit symmetrical.

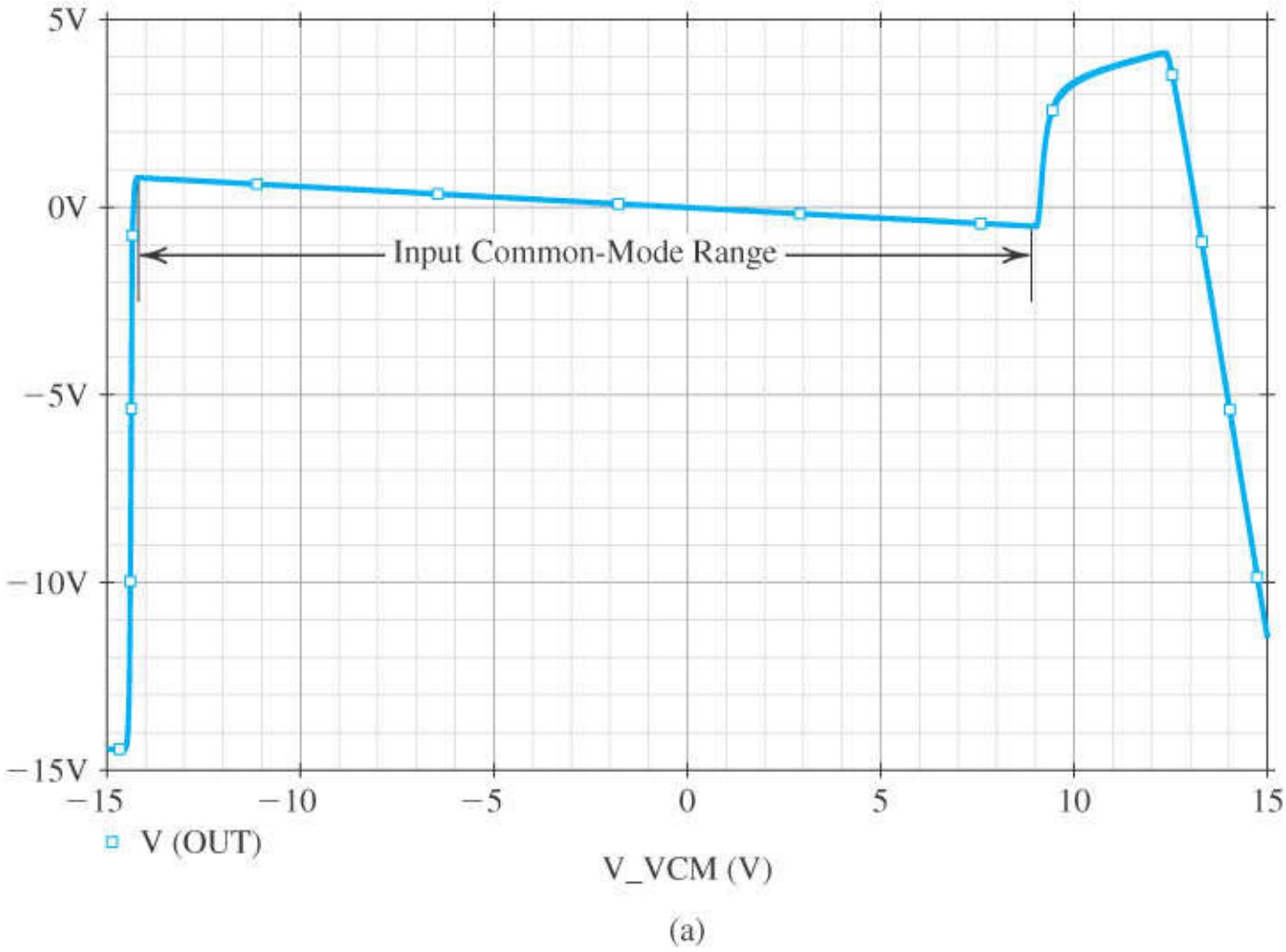

Figure 7.54 **(a)** The large-signal common-mode transfer characteristic of the op-amp circuit in Fig. 7.51. The differential input voltage v_d is set to –VOS = –260.4 μV to prevent premature saturation.

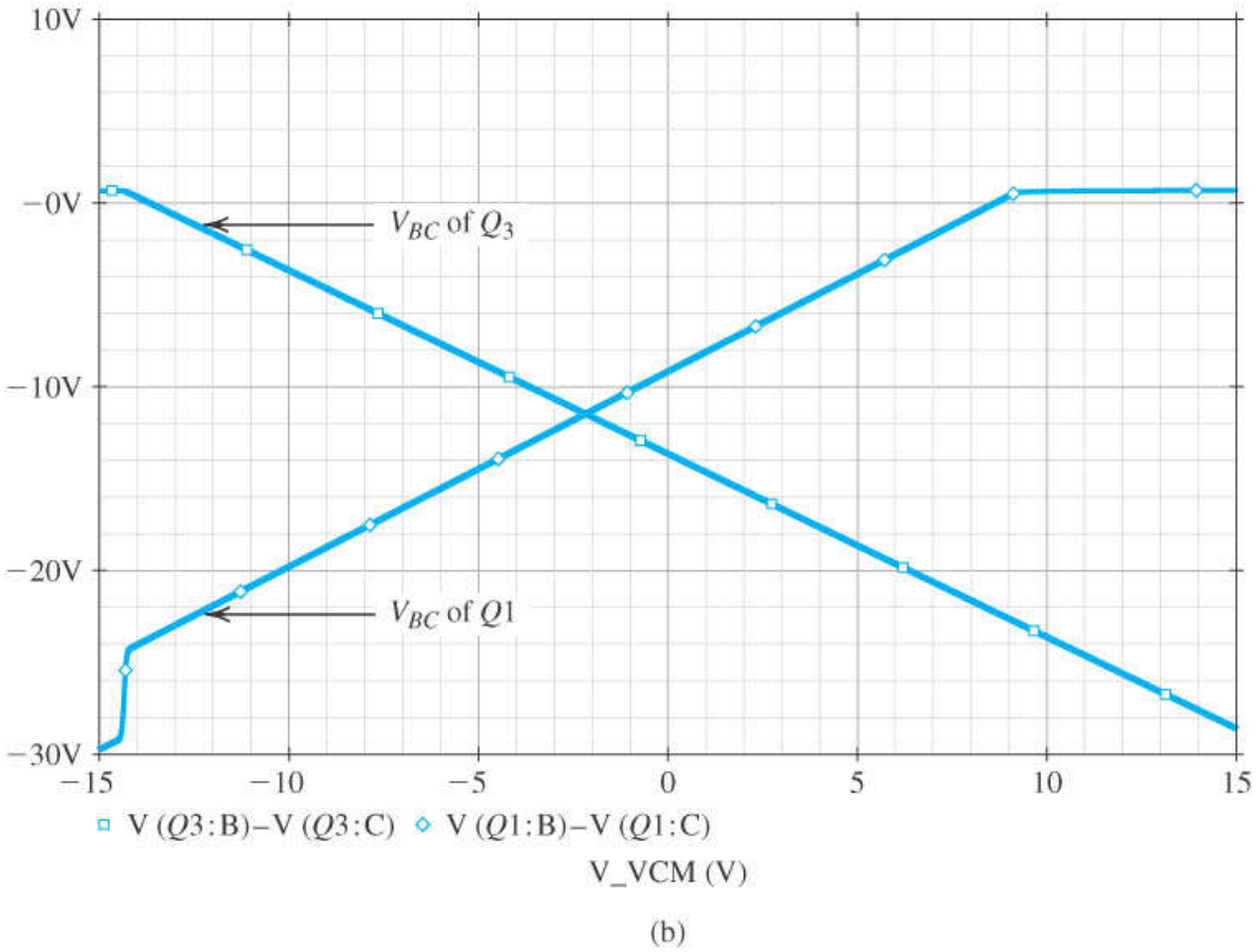

Figure 7.54 *(Continued)* **(b)** The effect of the common-mode input voltage VCM on the linearity of the input stage of the op-amp circuit in Fig. 7.51. The base–collector voltage of Q_1 and Q_3 is shown as a function of VCM. The input stage of the op-amp circuit leaves the active region when the base–collector junction of either Q_1 or Q_3 becomes forward biased (i.e., when VBC ≥ 0).

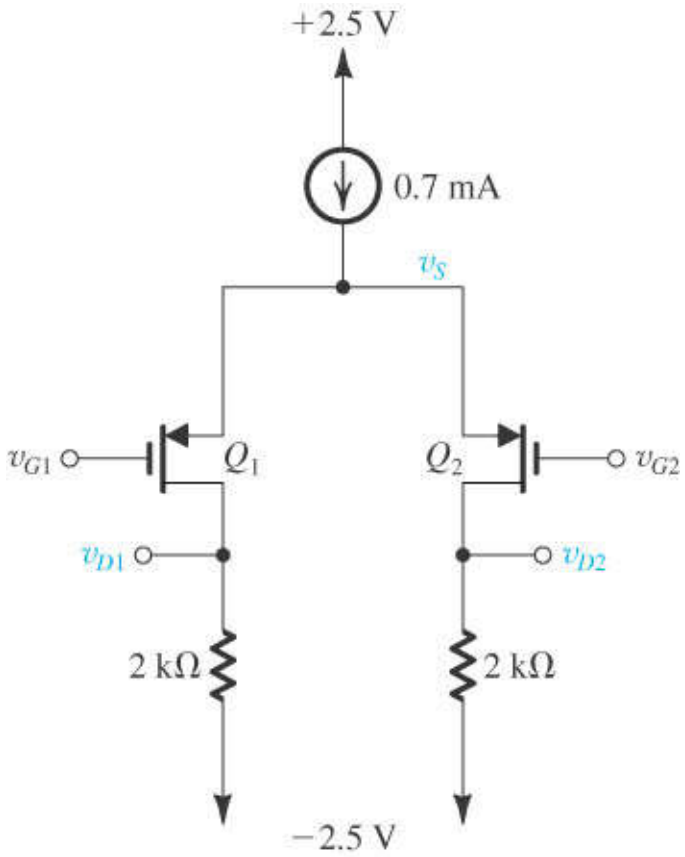

Figure P7.2

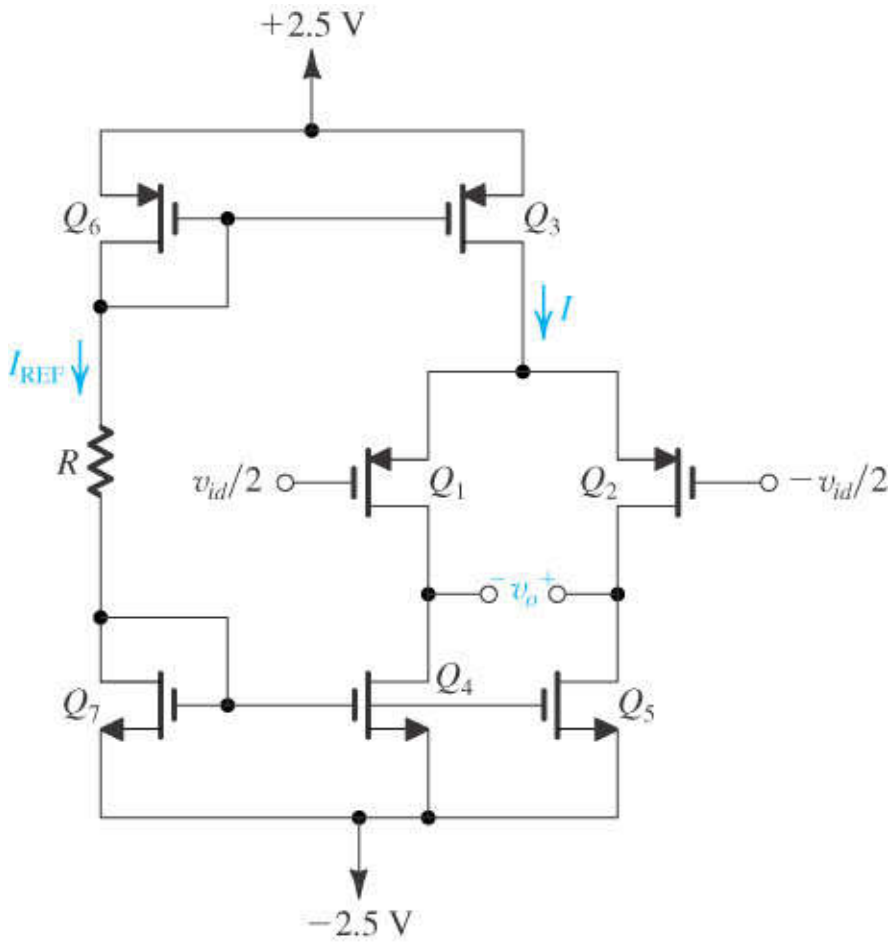

Figure P7.13

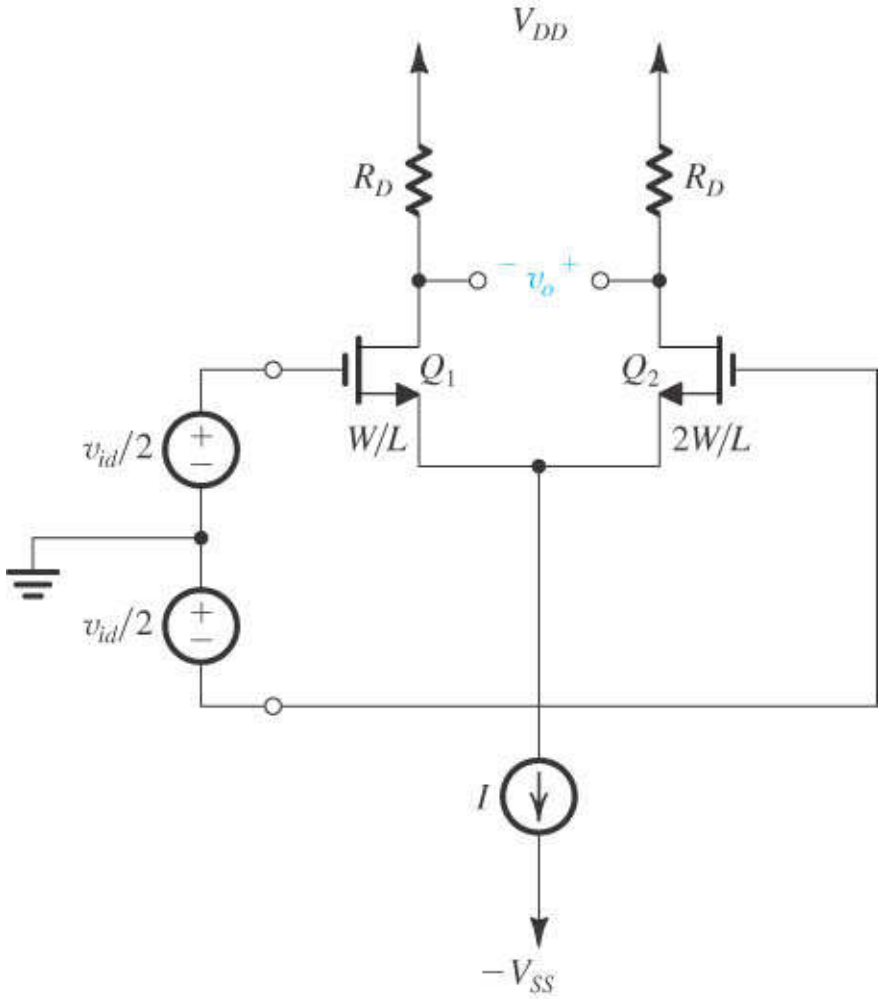

Figure P7.14

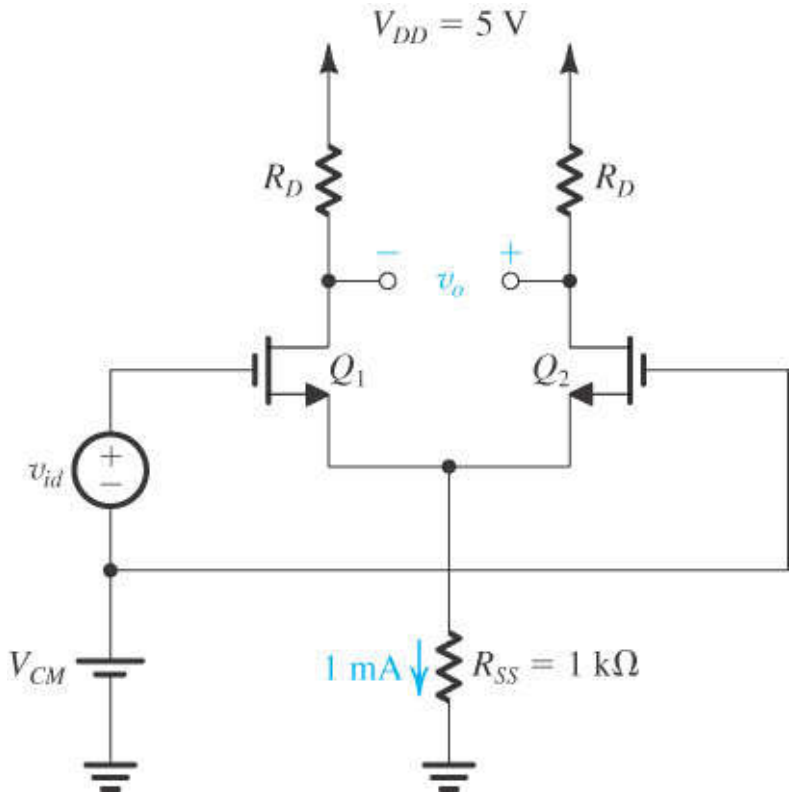

Figure P7.17

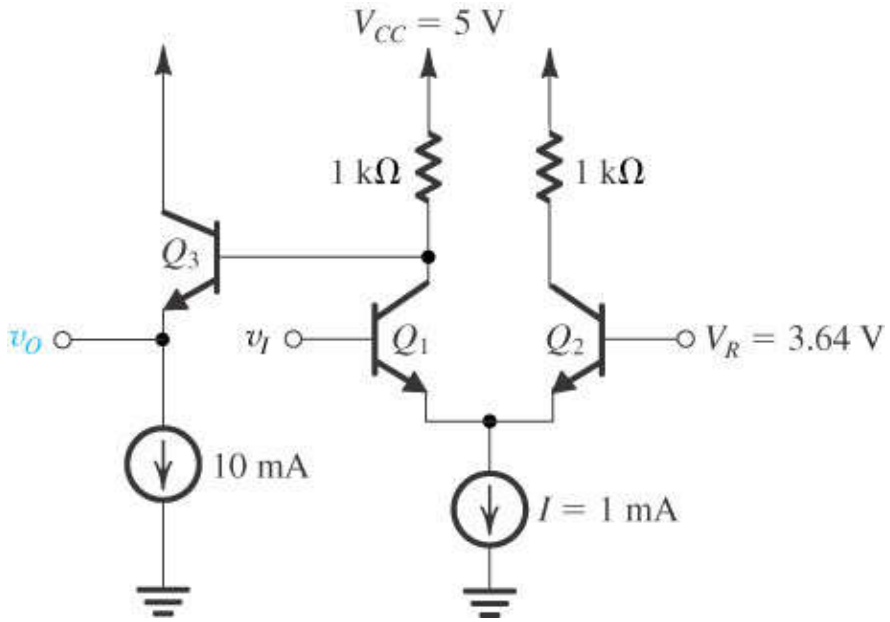

Figure P7.30

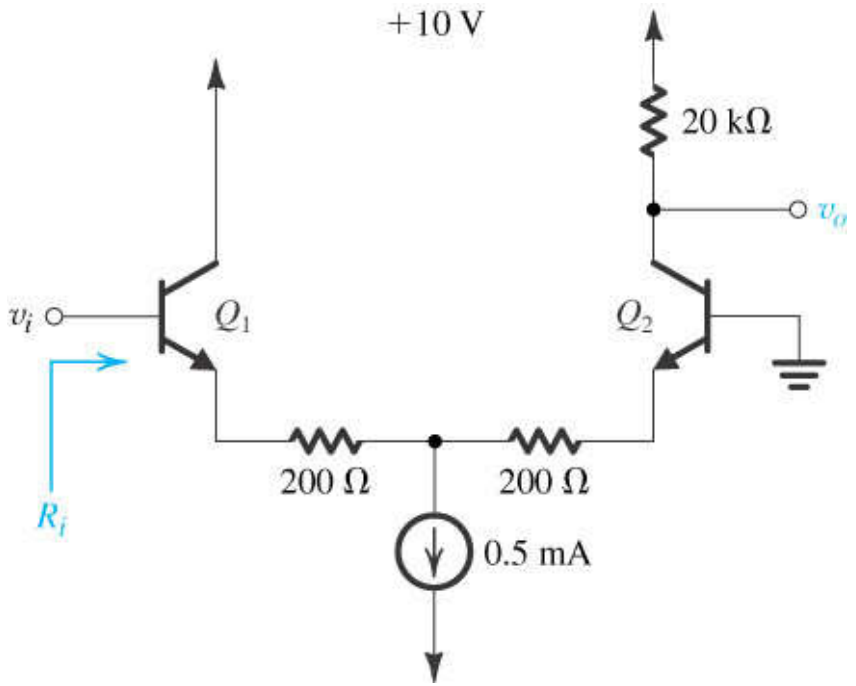

Figure P7.37

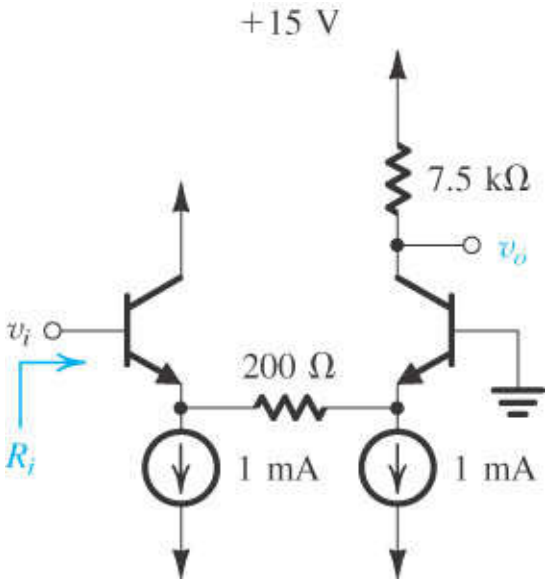

Figure P7.38

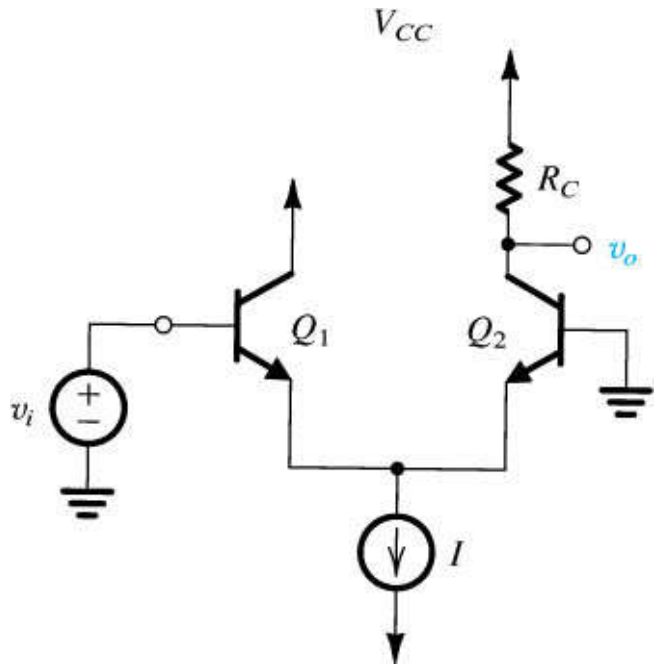

Figure P7.39

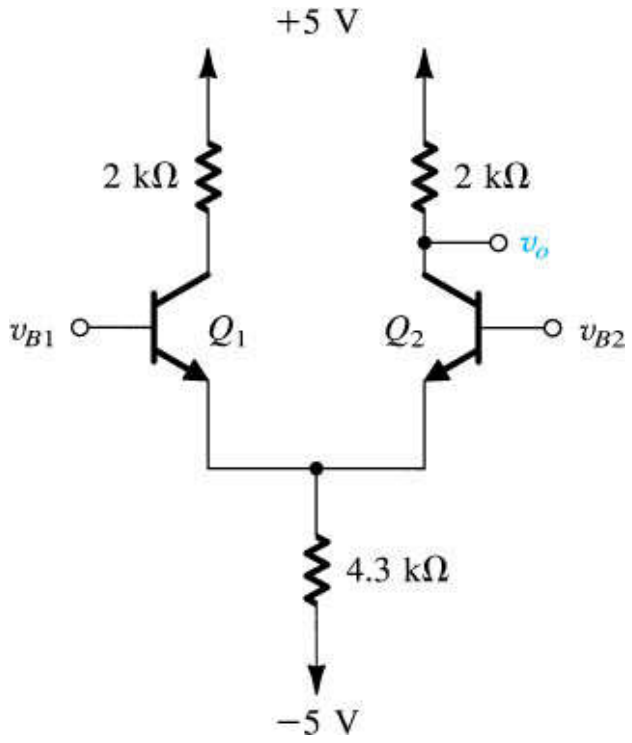

Figure P7.40

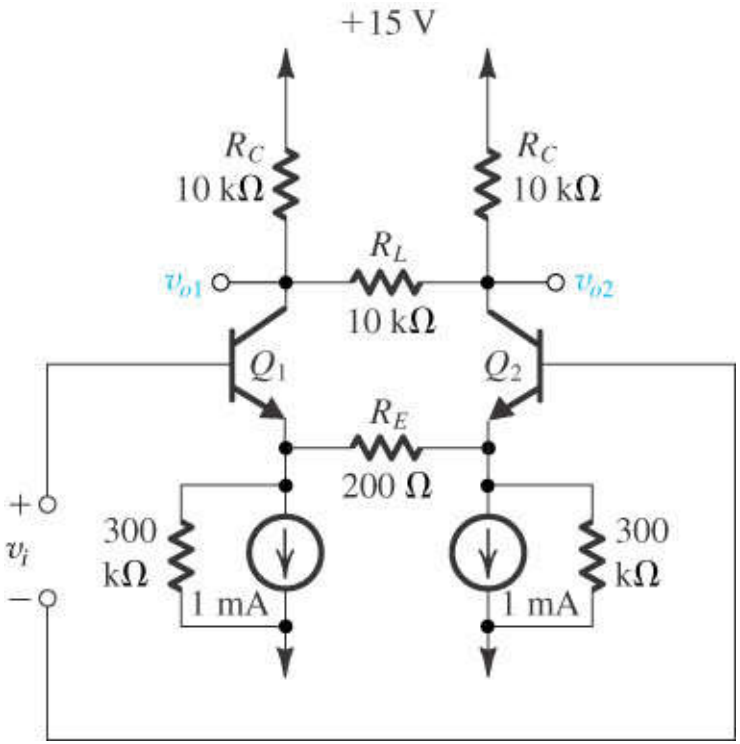

Figure P7.41

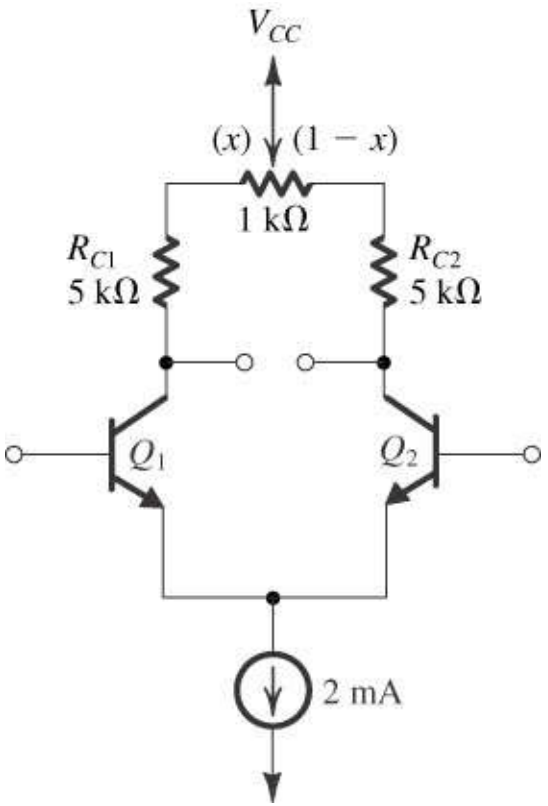

Figure P7.57

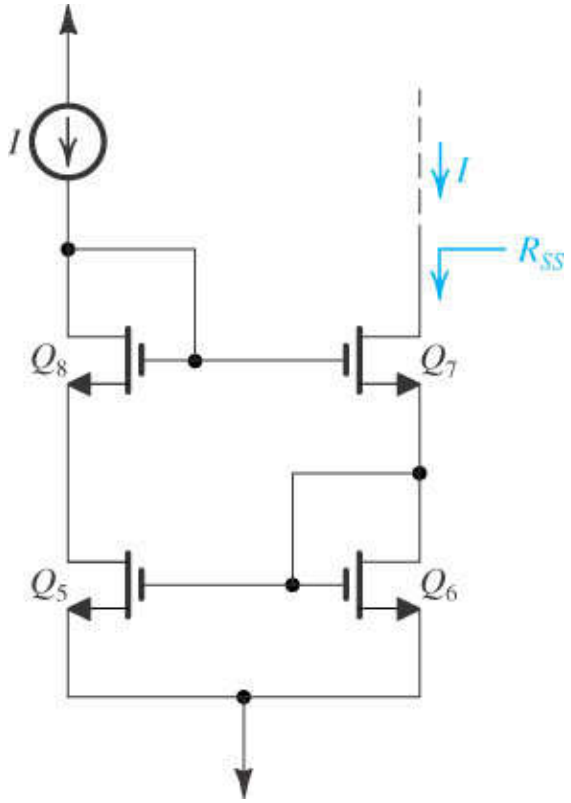

Figure P7.64

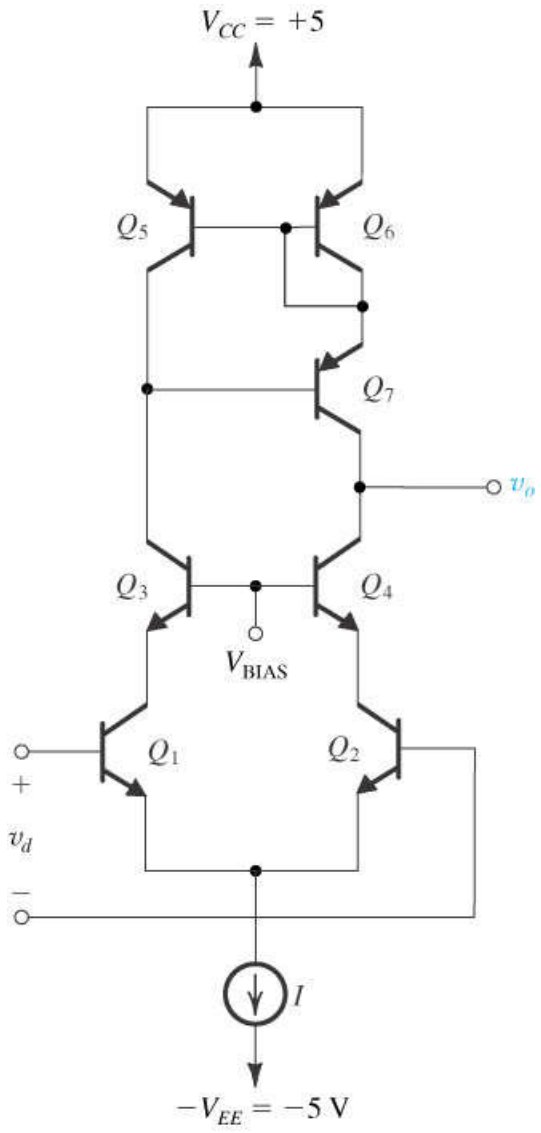

Figure P7.74

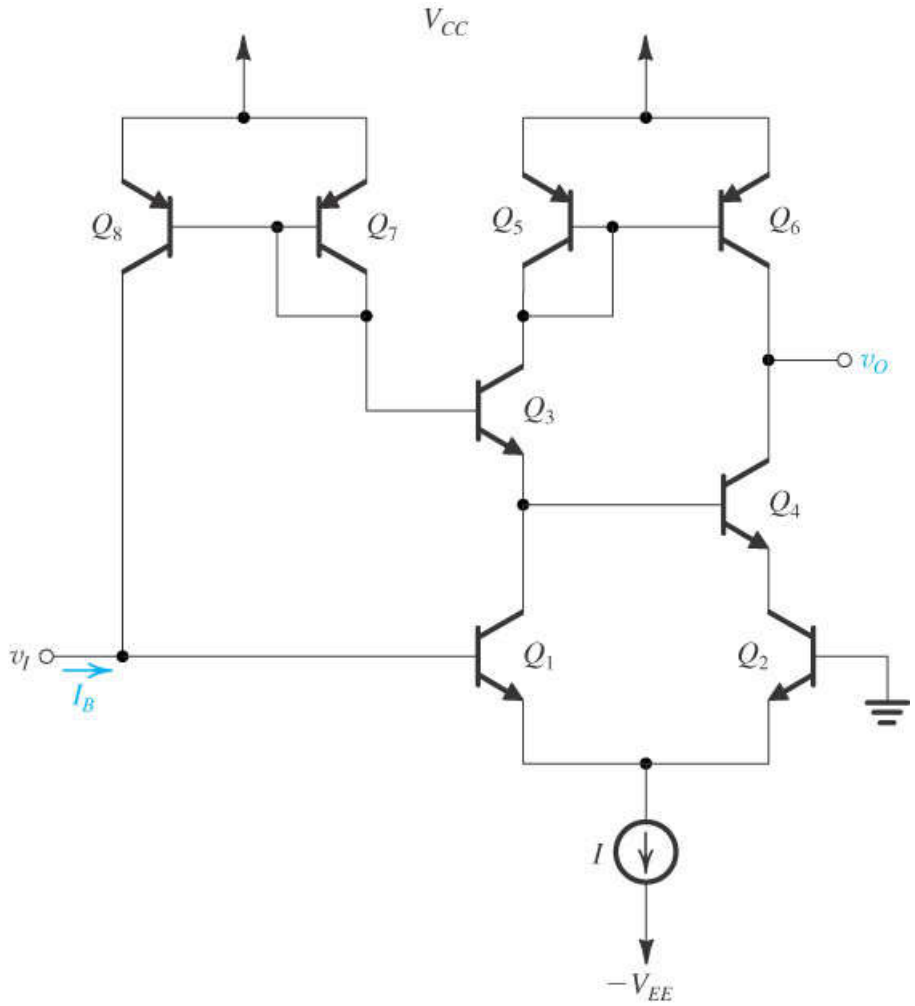

Figure P7.76

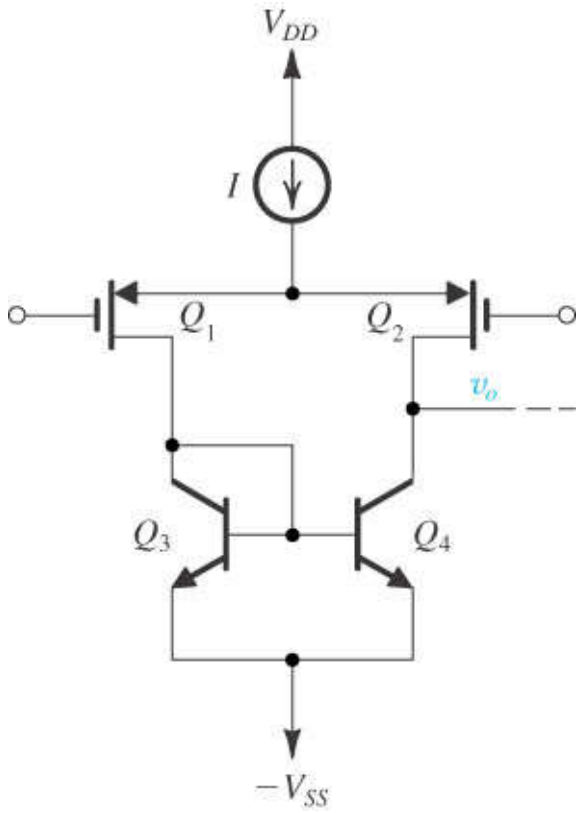

Figure P7.79

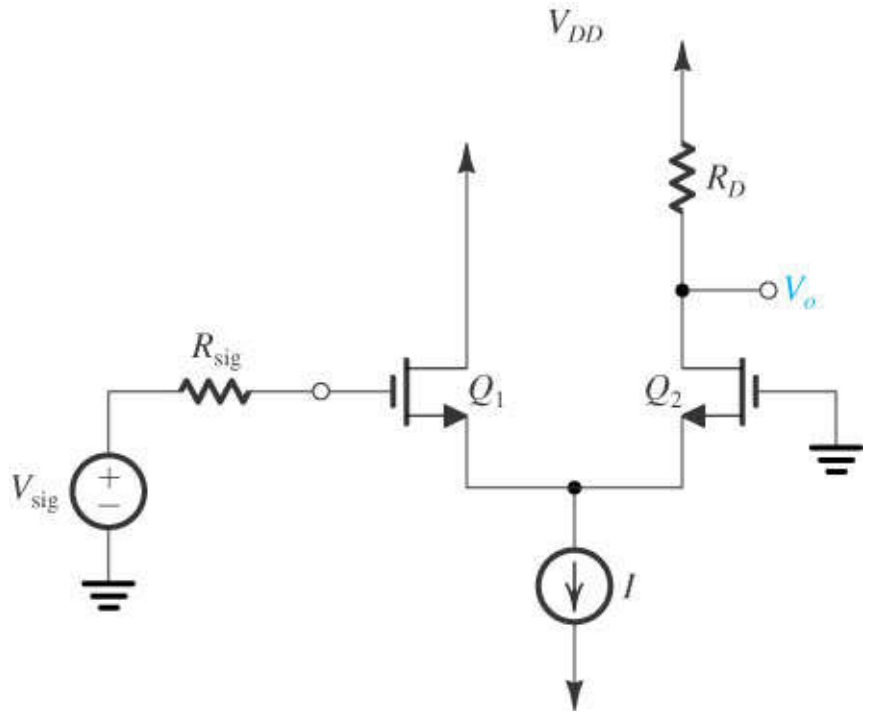

Figure P7.88

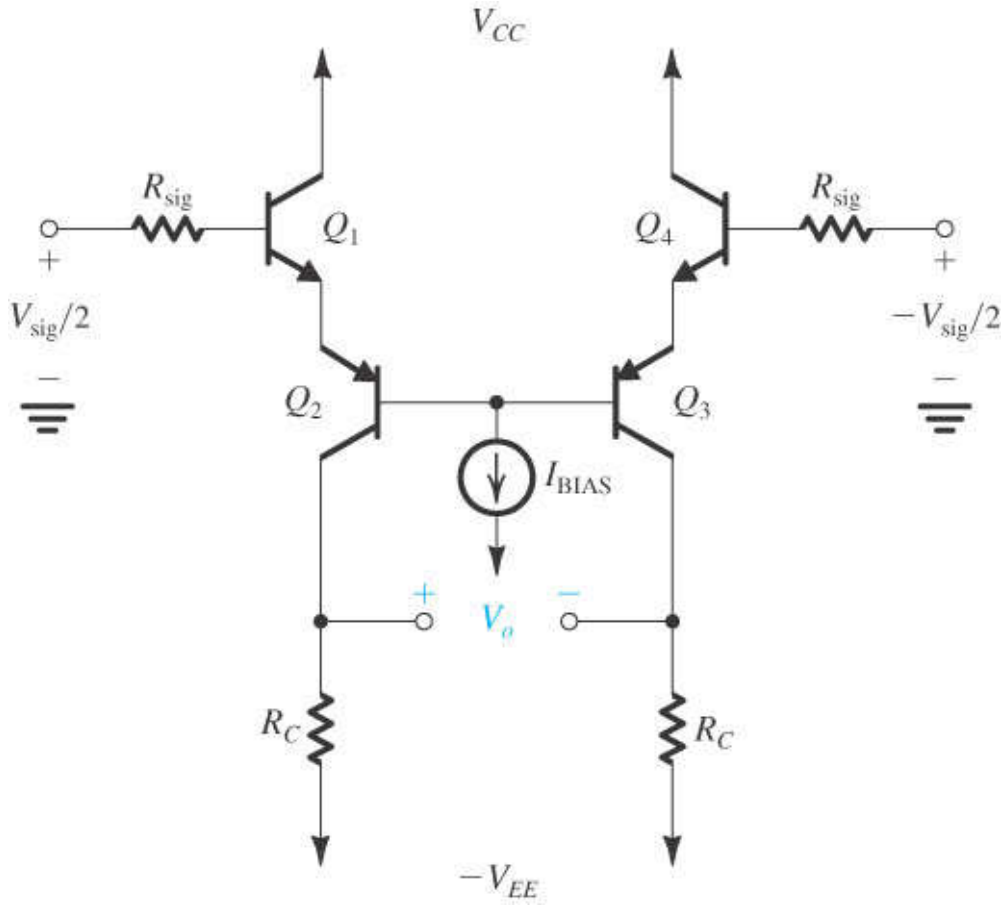

Figure P7.89

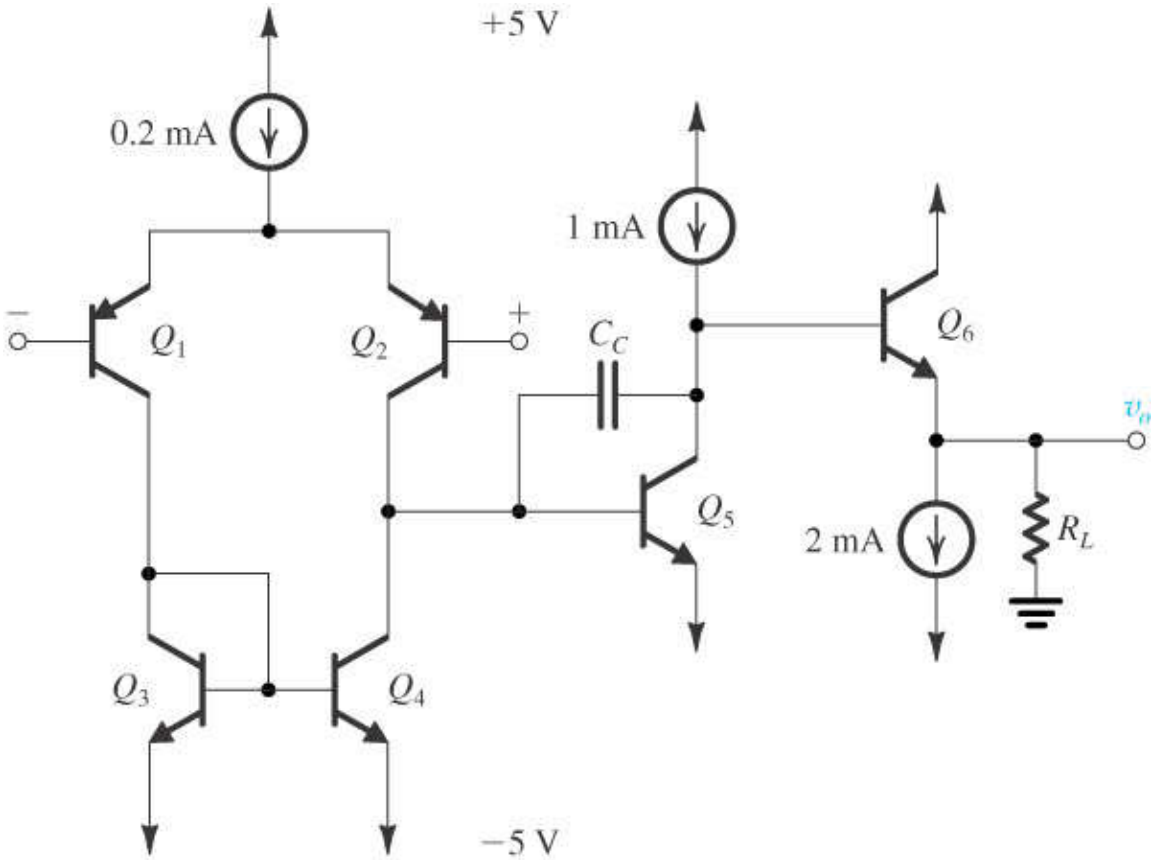

Figure P7.95

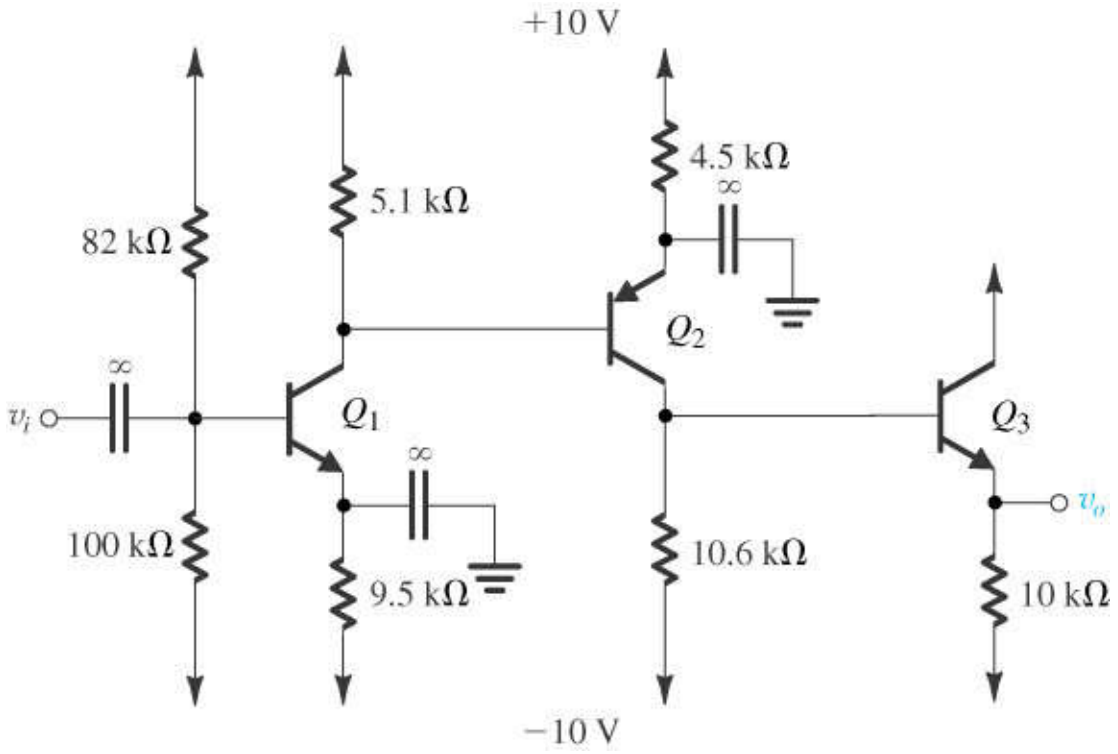

Figure P7.101

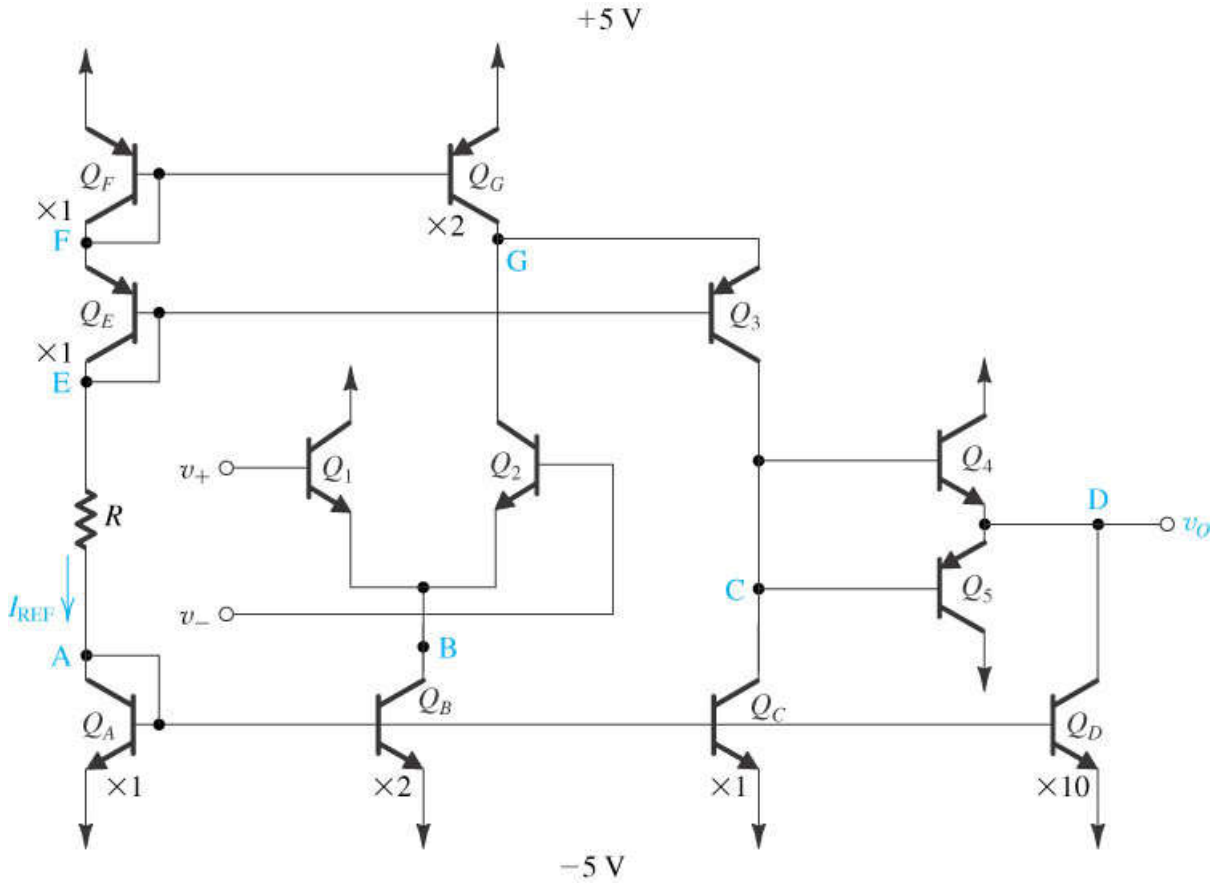

Figure P7.102

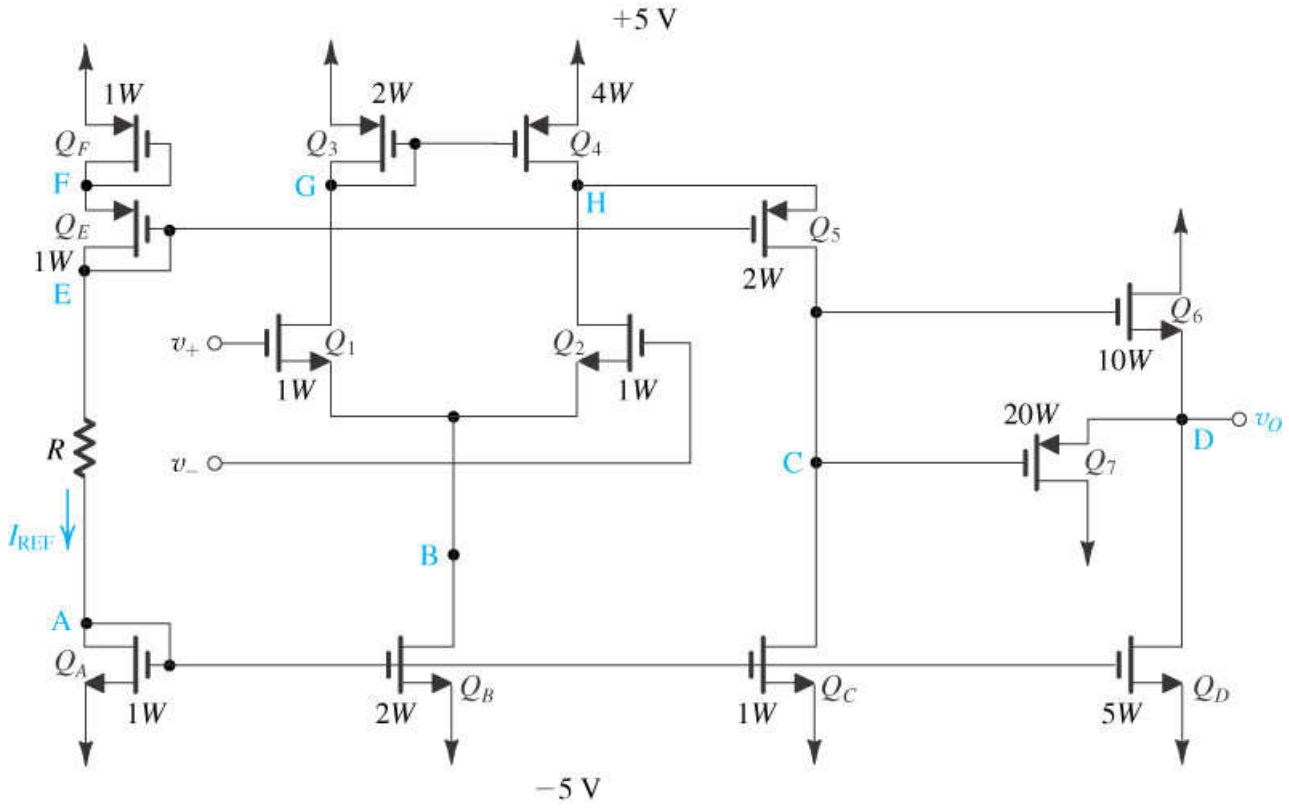

Figure P7.103