Diodes

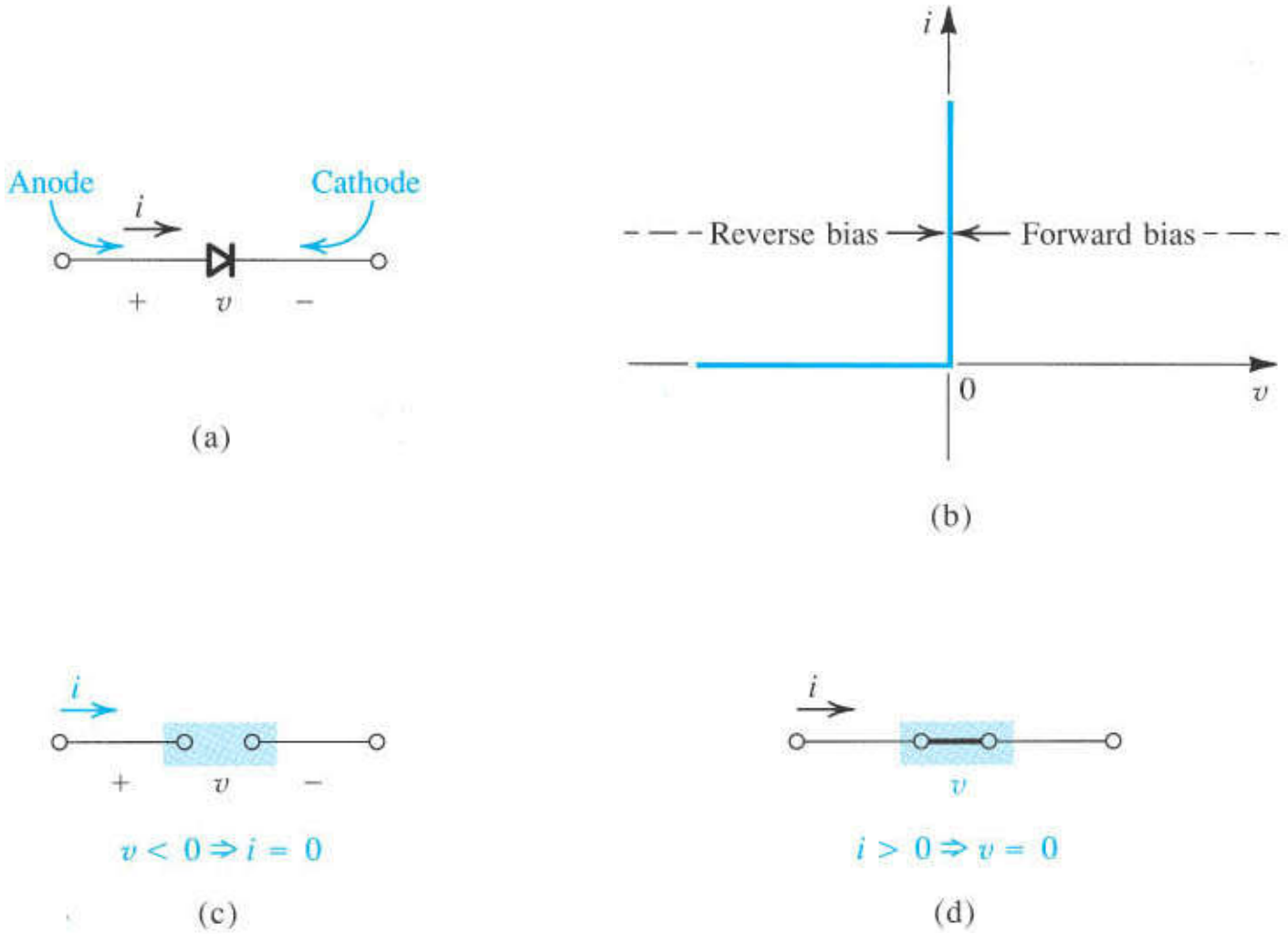


Figure 3.1 The ideal diode: **(a)** diode circuit symbol; **(b)** *i*–*v* characteristic; **(c)** equivalent circuit in the reverse direction; **(d)** equivalent circuit in the forward direction.

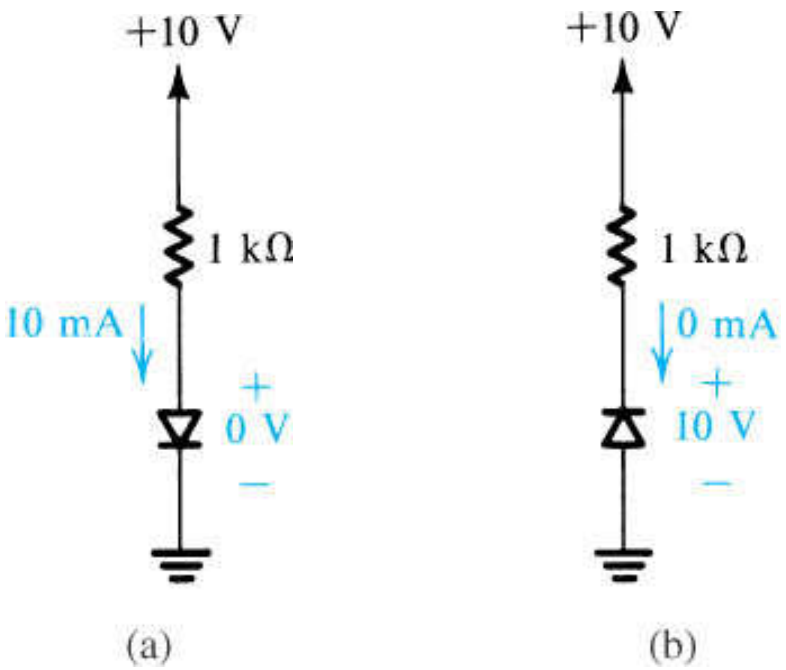


Figure 3.2 The two modes of operation of ideal diodes and the use of an external circuit to limit the forward current **(a)** and the reverse voltage **(b)**.

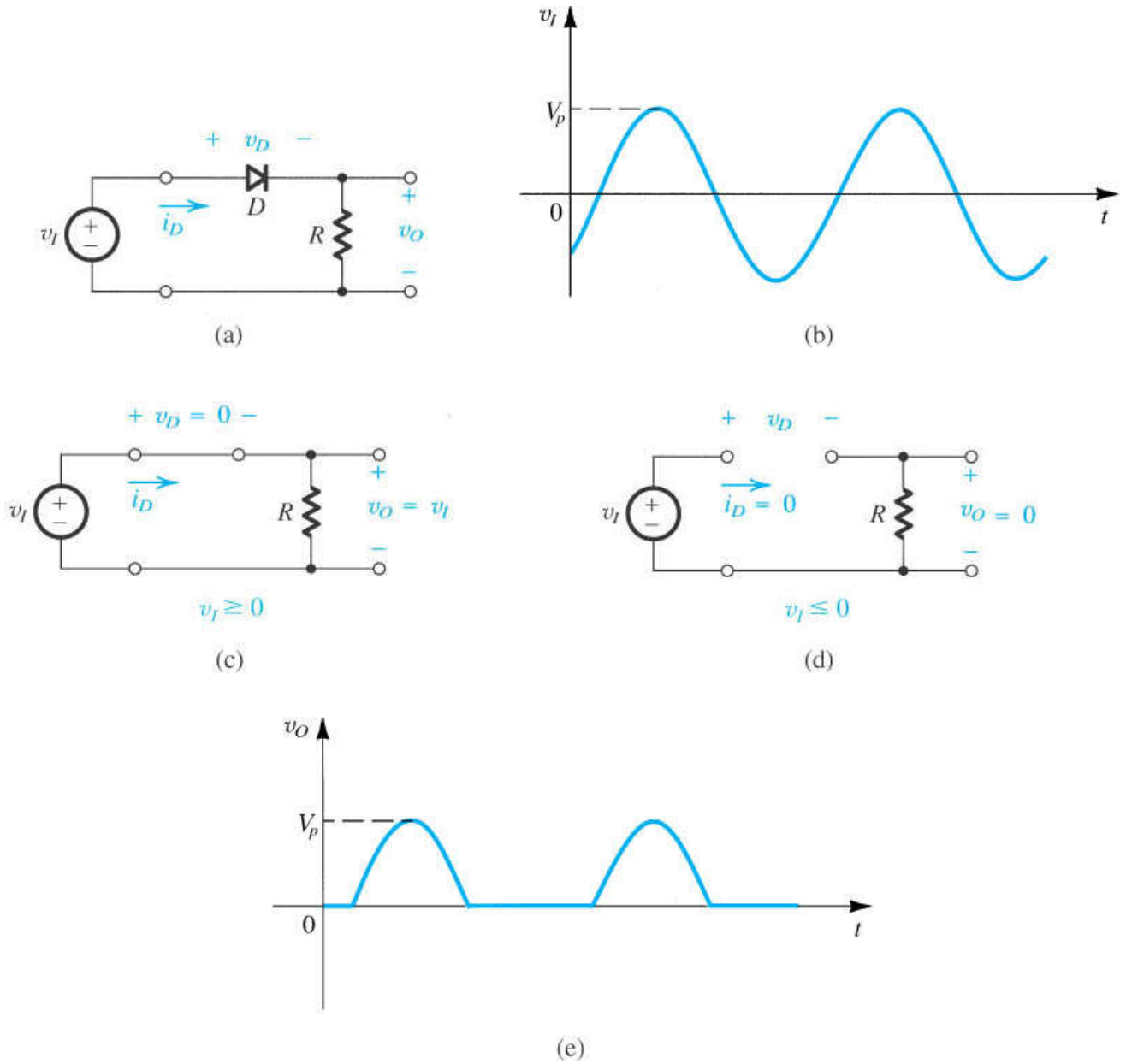


Figure 3.3 **(a)** Rectifier circuit. **(b)** Input waveform. **(c)** Equivalent circuit when $v_I \geq 0$. **(d)** Equivalent circuit when v_I ✧ 0. **(e)** Output waveform.

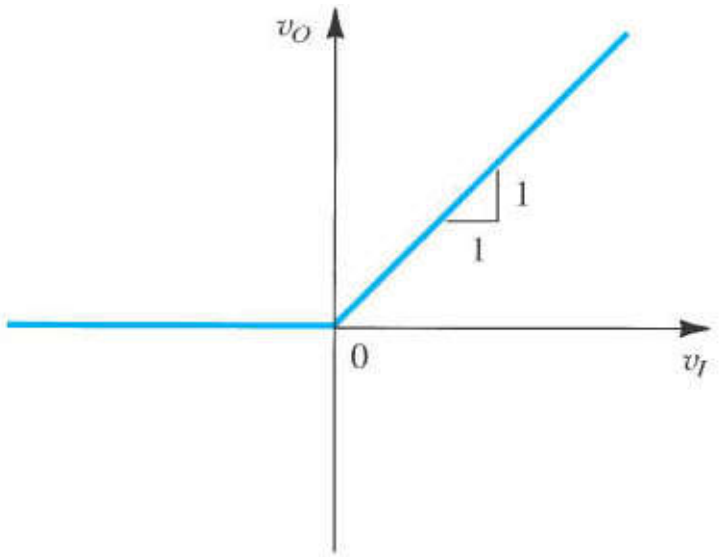


Figure E3.1

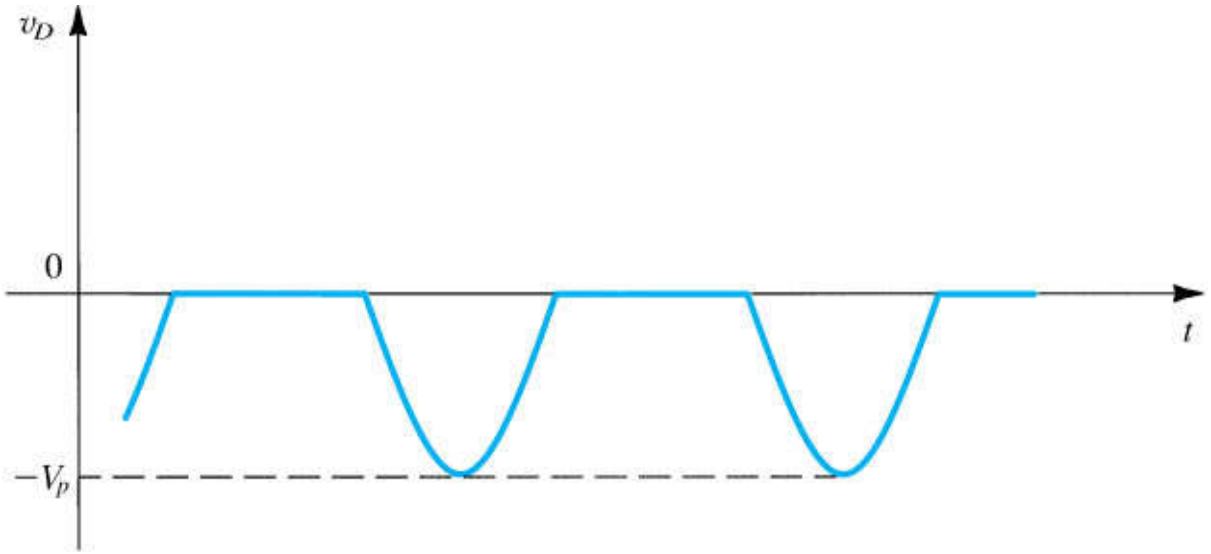


Figure E3.2

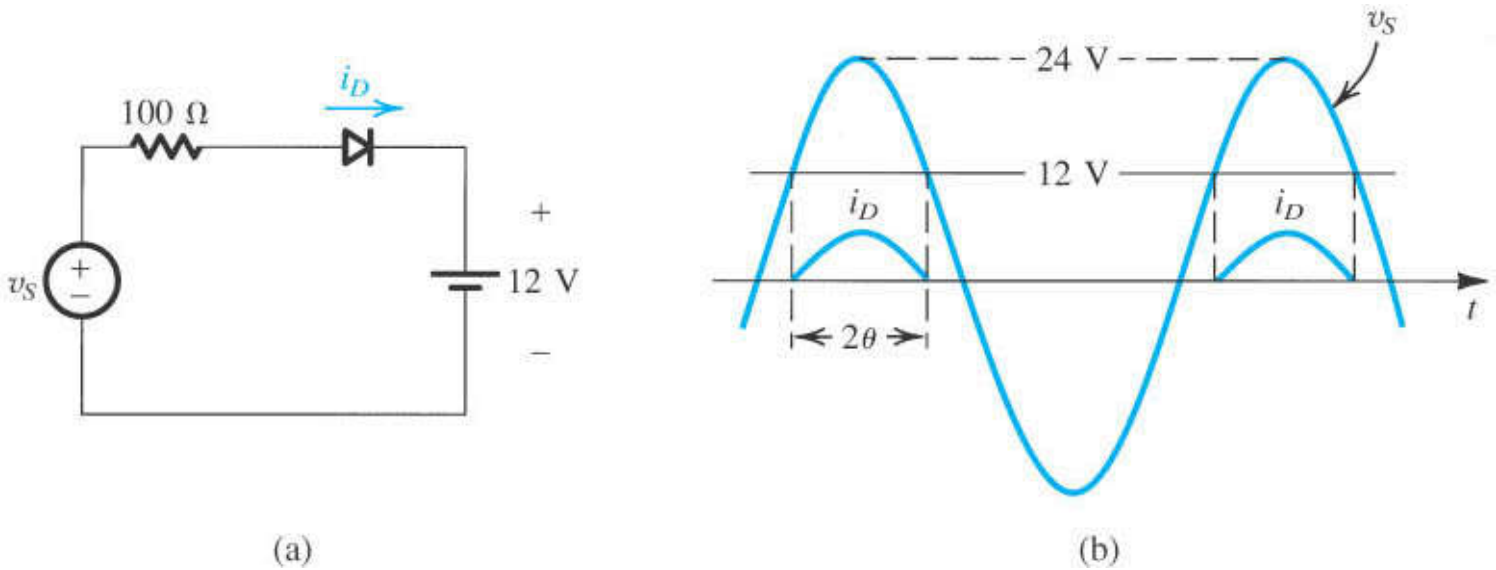


Figure 3.4 Circuit and waveforms for Example 3.1.

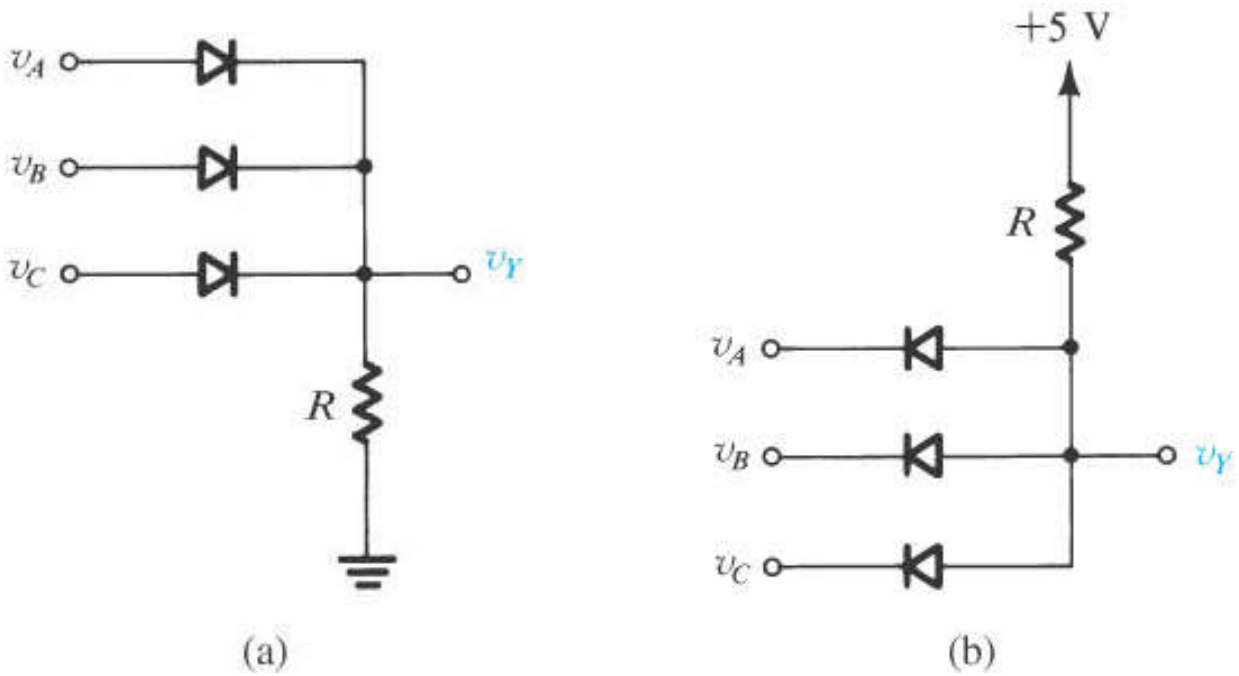


Figure 3.5 Diode logic gates: **(a)** OR gate; **(b)** AND gate (in a positive-logic system).

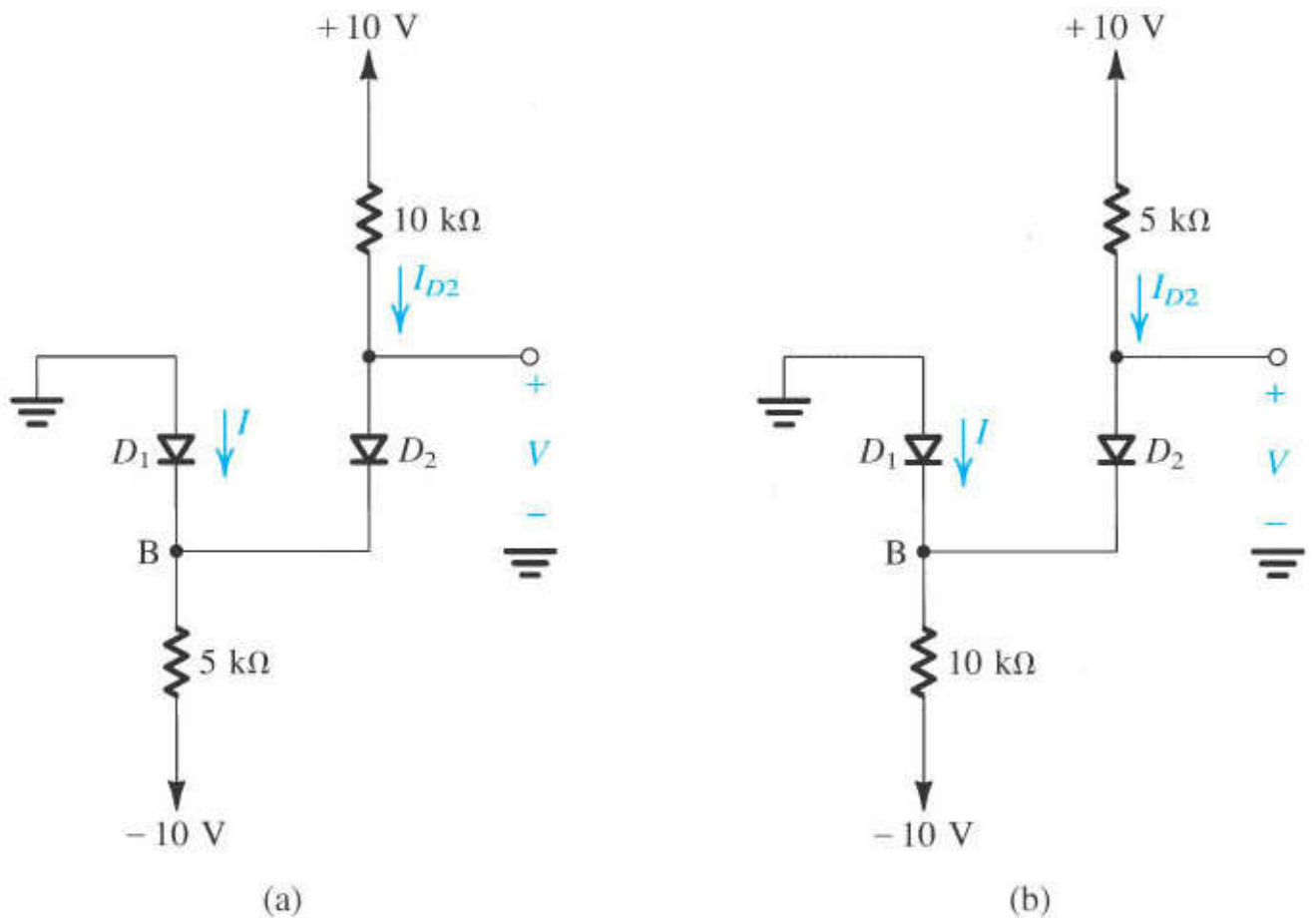


Figure 3.6 Circuits for Example 3.2.

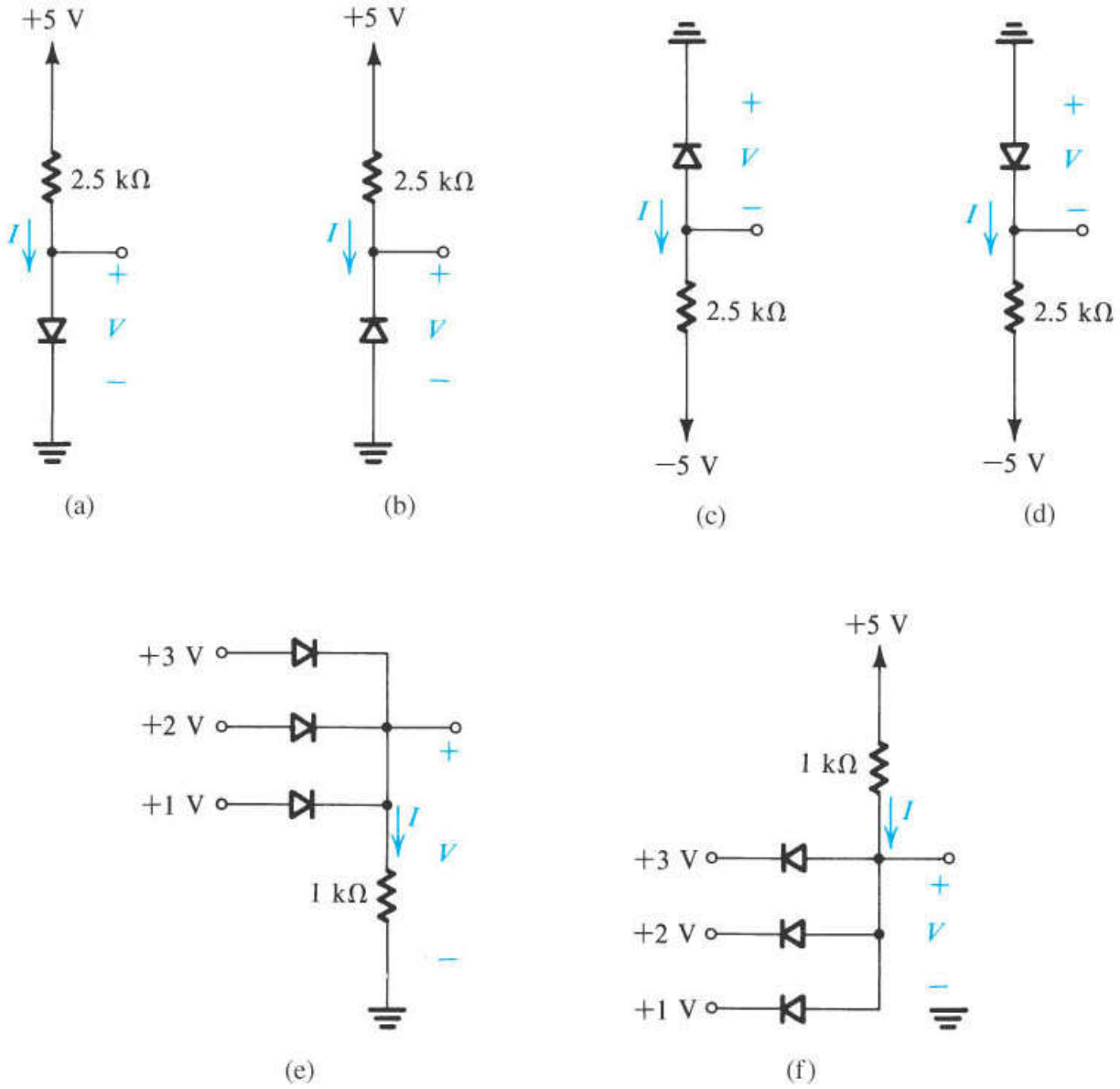


Figure E3.4

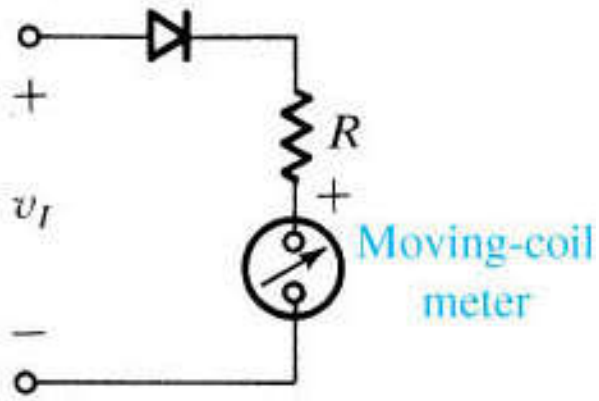


Figure E3.5

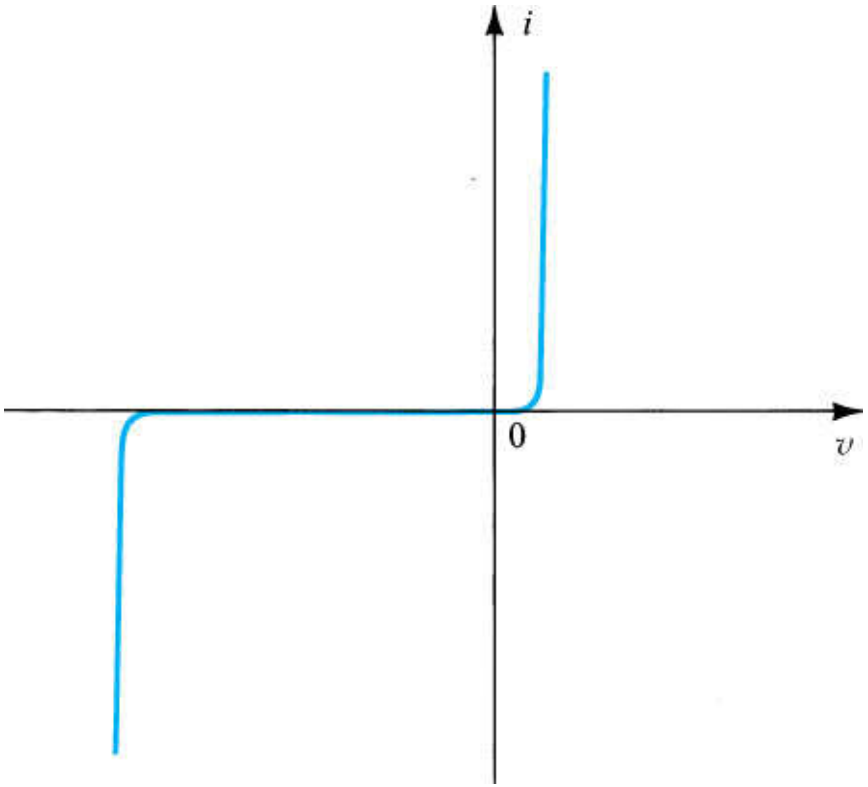


Figure 3.7 The *i–v* characteristic of a silicon junction diode.

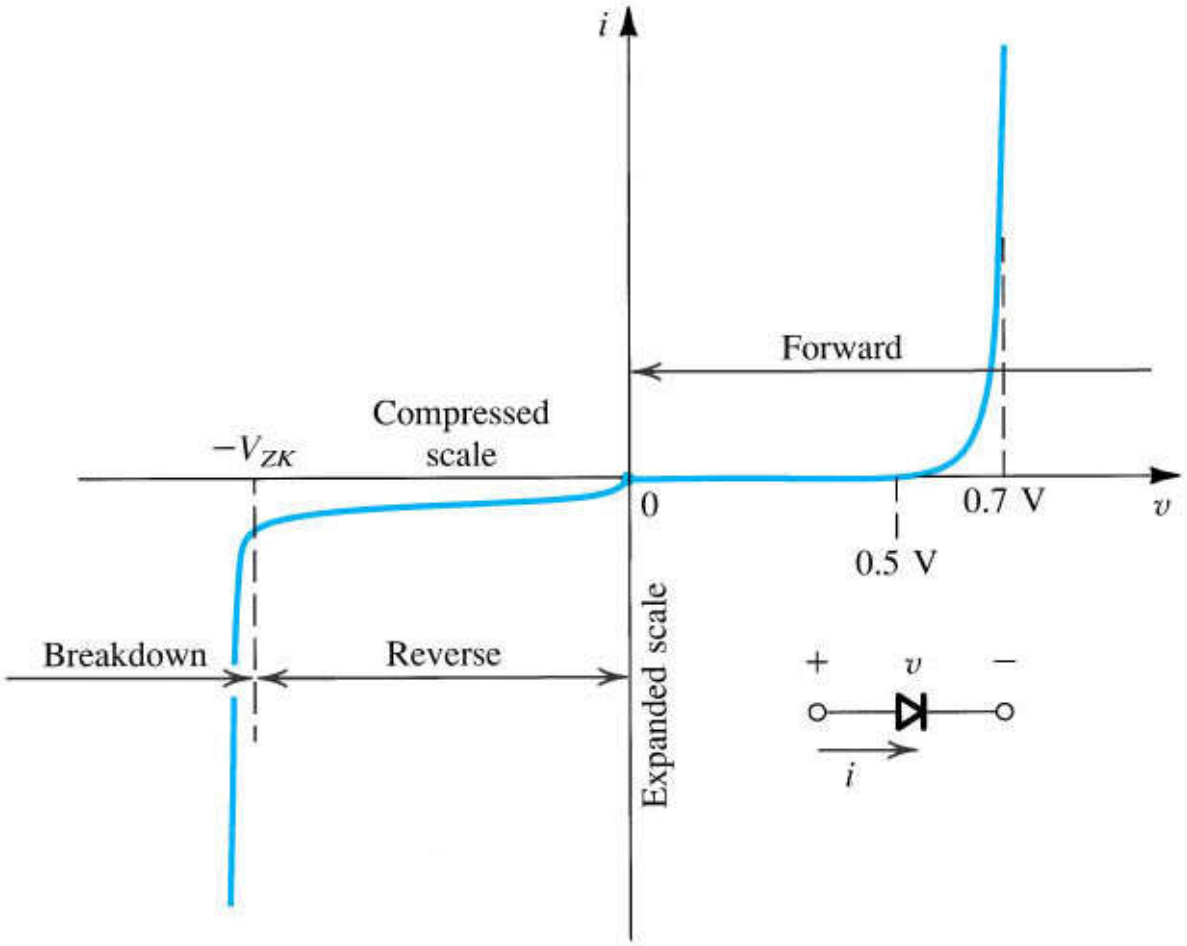


Figure 3.8 The diode *i–v* relationship with some scales expanded and others compressed in order to reveal details.

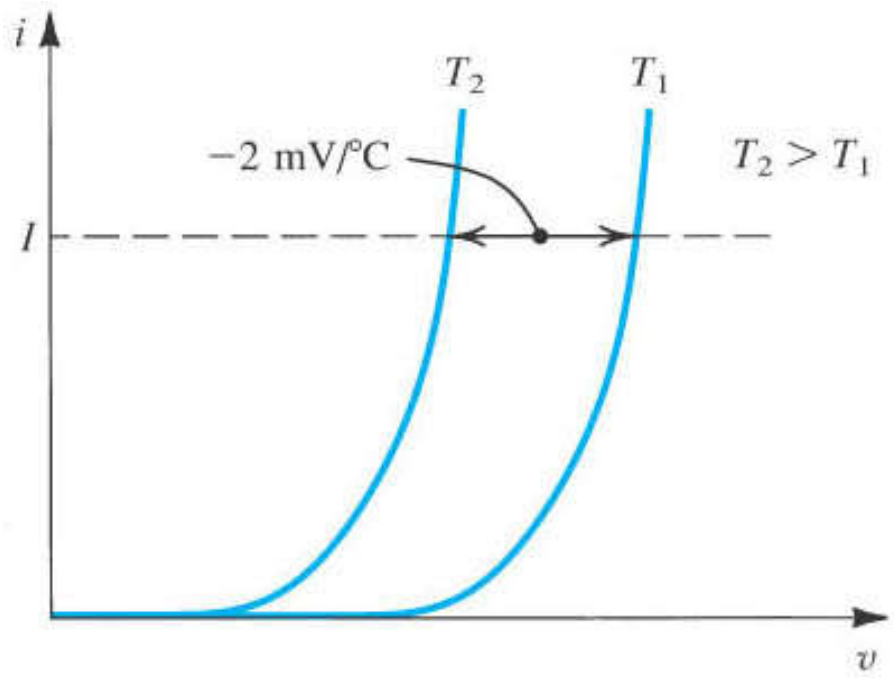


Figure 3.9 Illustrating the temperature dependence of the diode forward characteristic. At a constant current, the voltage drop decreases by approximately 2 mV for every 1°C increase in temperature.

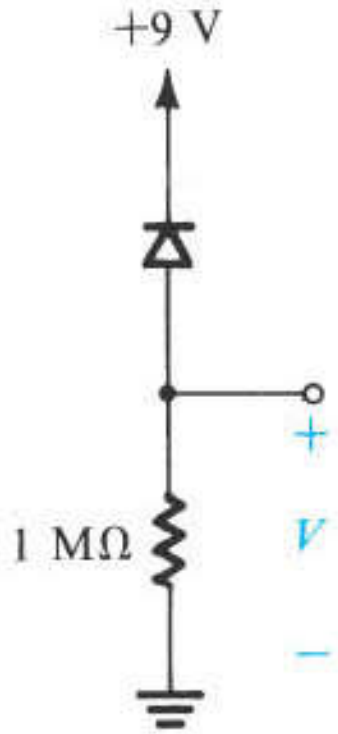


Figure E3.9

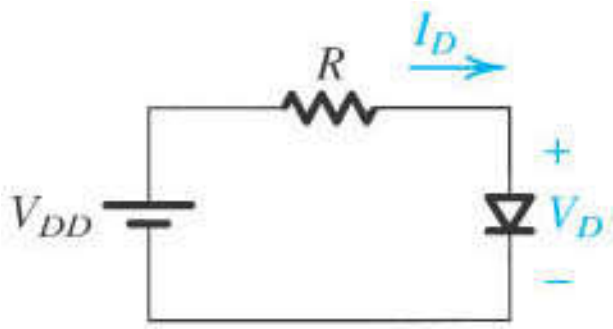


Figure 3.10 A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting.

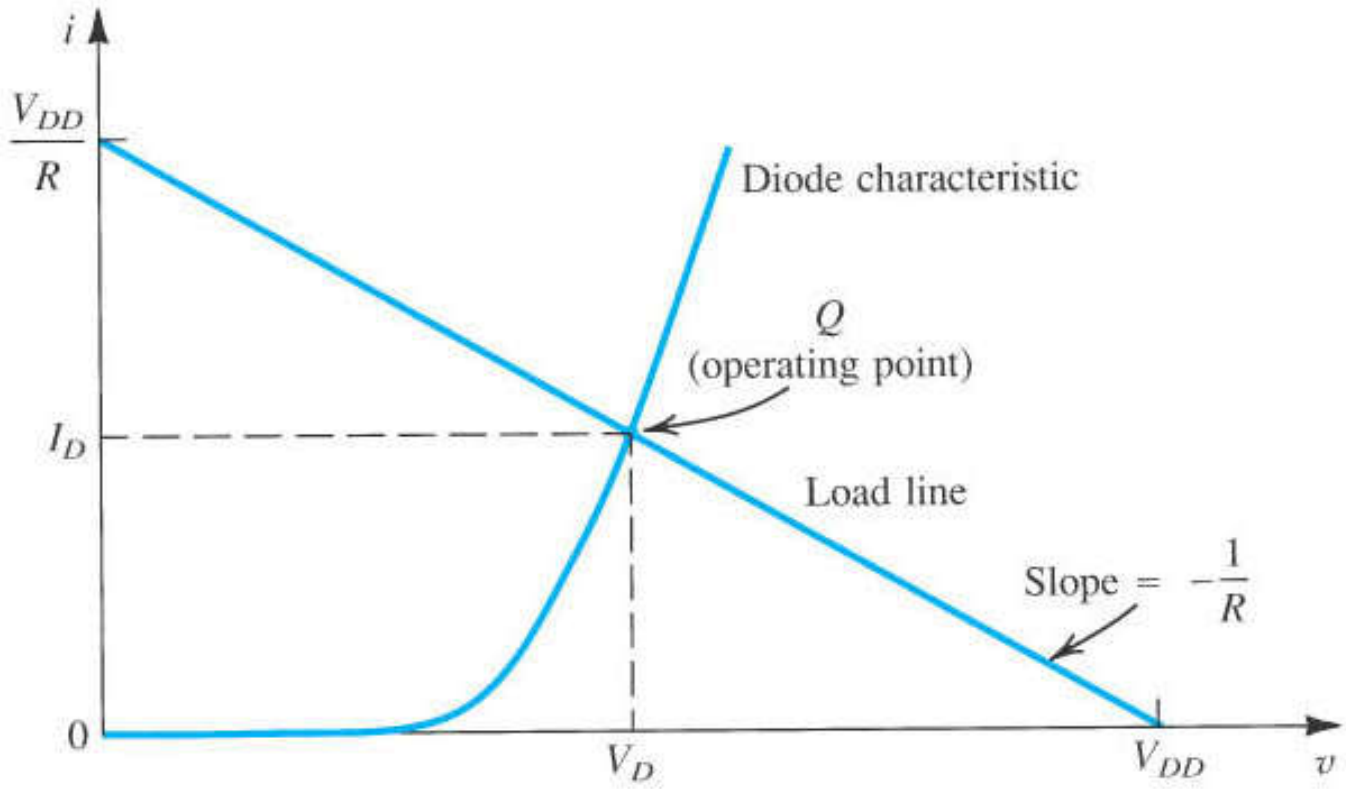


Figure 3.11 Graphical analysis of the circuit in Fig. 3.10 using the exponential diode model.

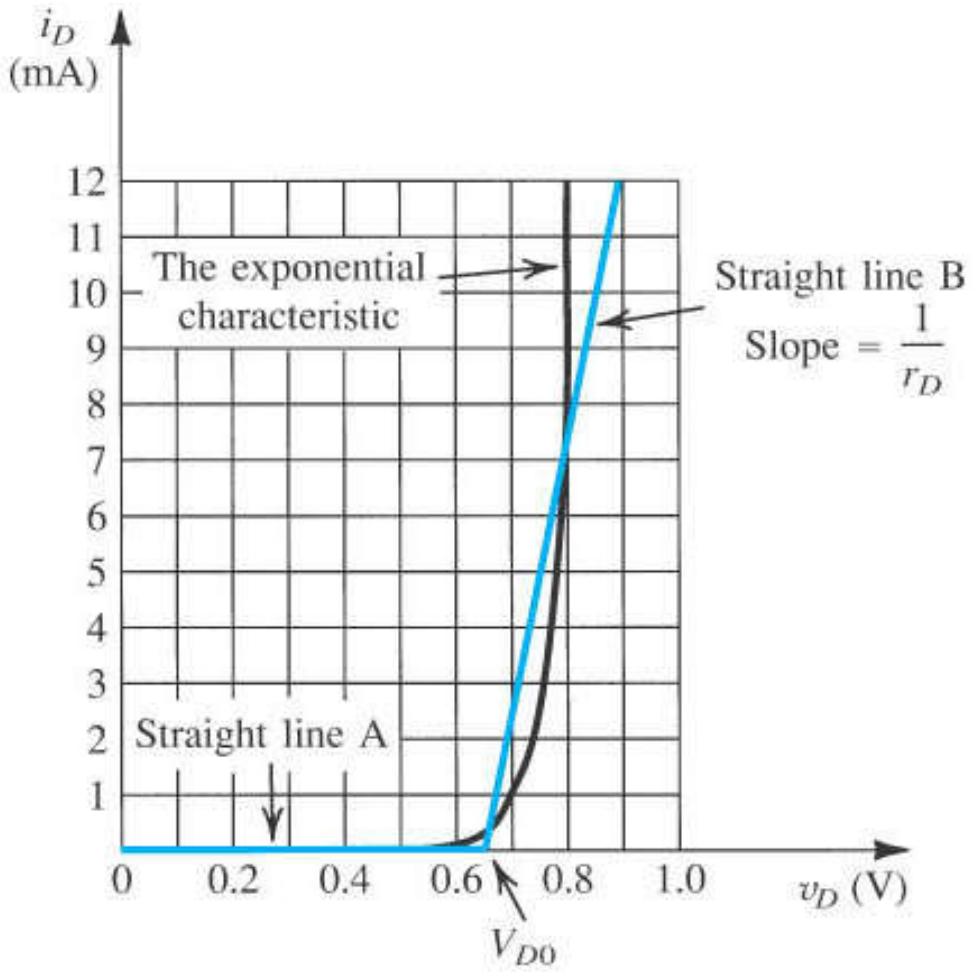


Figure 3.12 Approximating the diode forward characteristic with two straight lines: the piecewise-linear model.

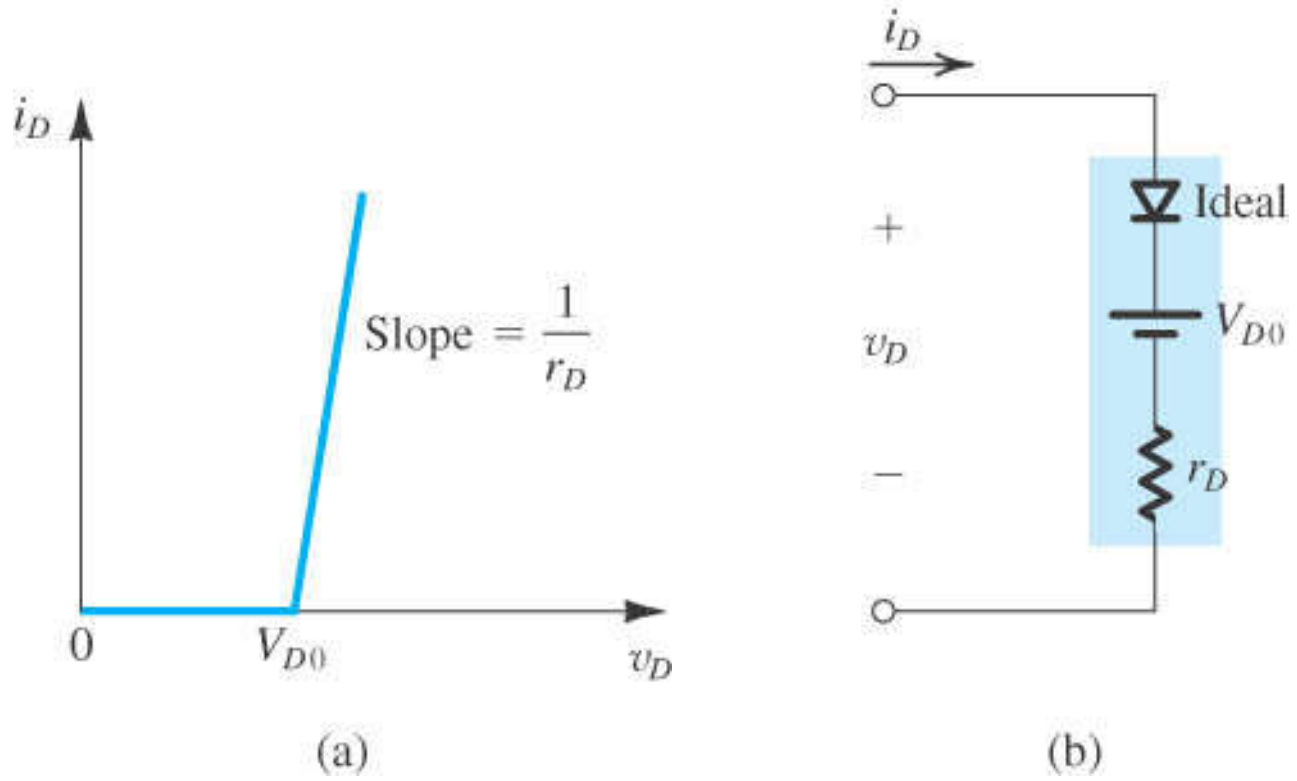


Figure 3.13 Piecewise-linear model of the diode forward characteristic and its equivalent circuit representation.

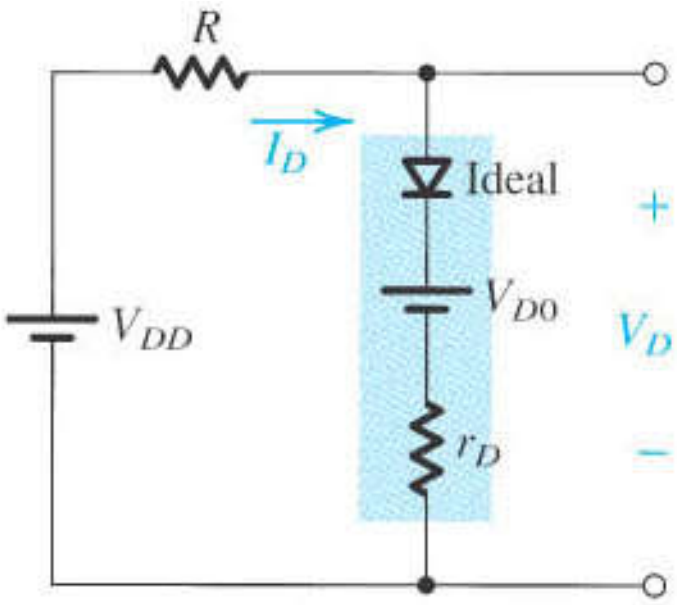


Figure 3.14 The circuit of Fig. 3.10 with the diode replaced with its piecewise-linear model of Fig. 3.13.

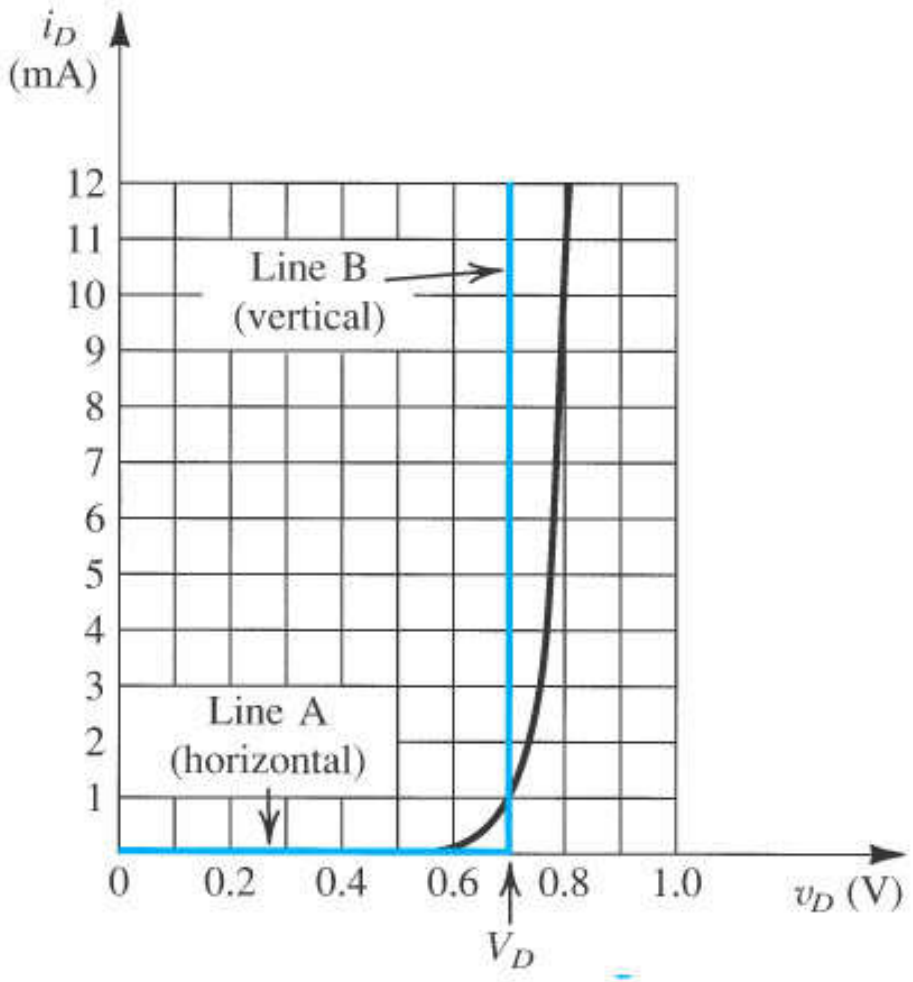


Figure 3.15 Development of the constant-voltage-drop model of the diode forward characteristics. A vertical straight line (B) is used to approximate the fast-rising exponential. Observe that this simple model predicts V_D to within ±0.1 V over the current range of 0.1 mA to 10 mA.

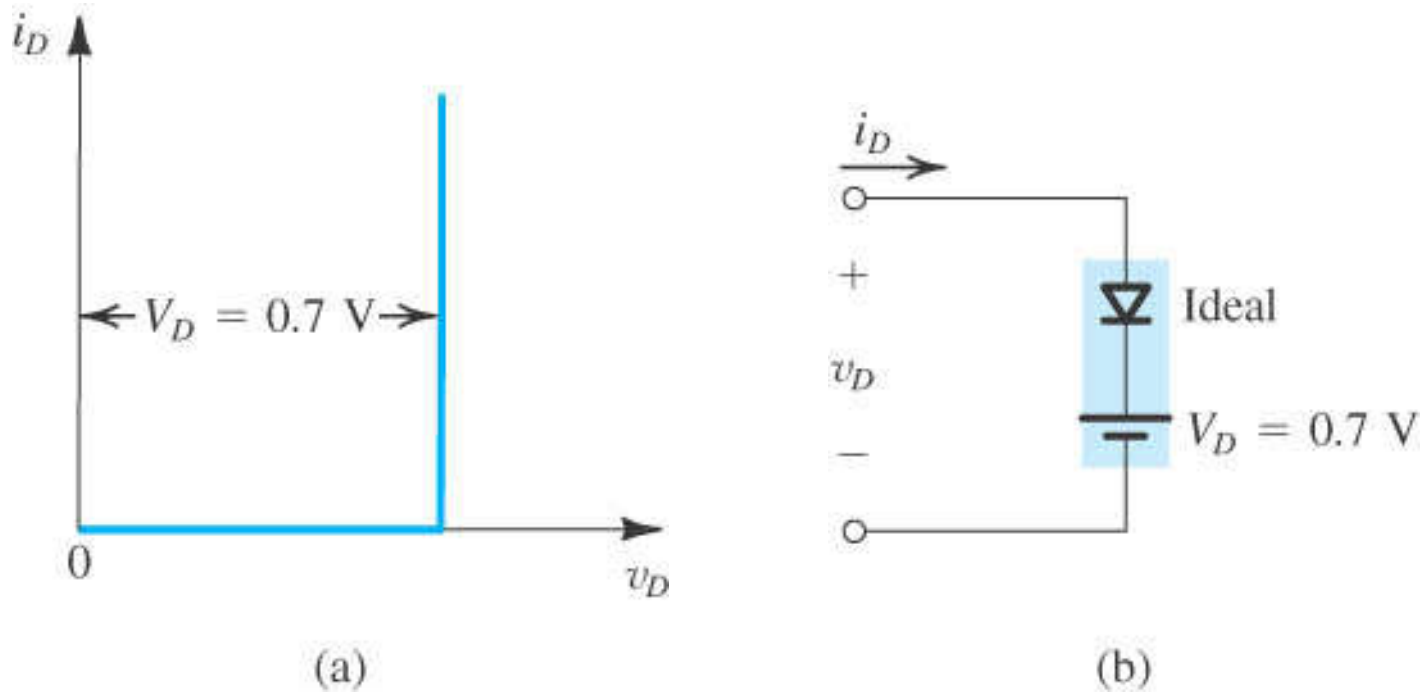


Figure 3.16 The constant-voltage-drop model of the diode forward characteristics and its equivalent-circuit representation.

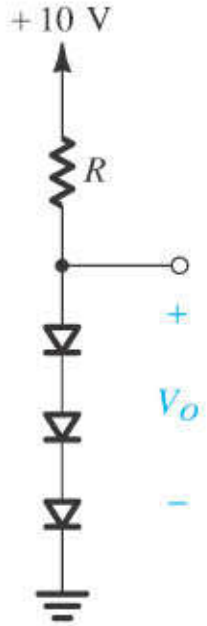


Figure E3.12

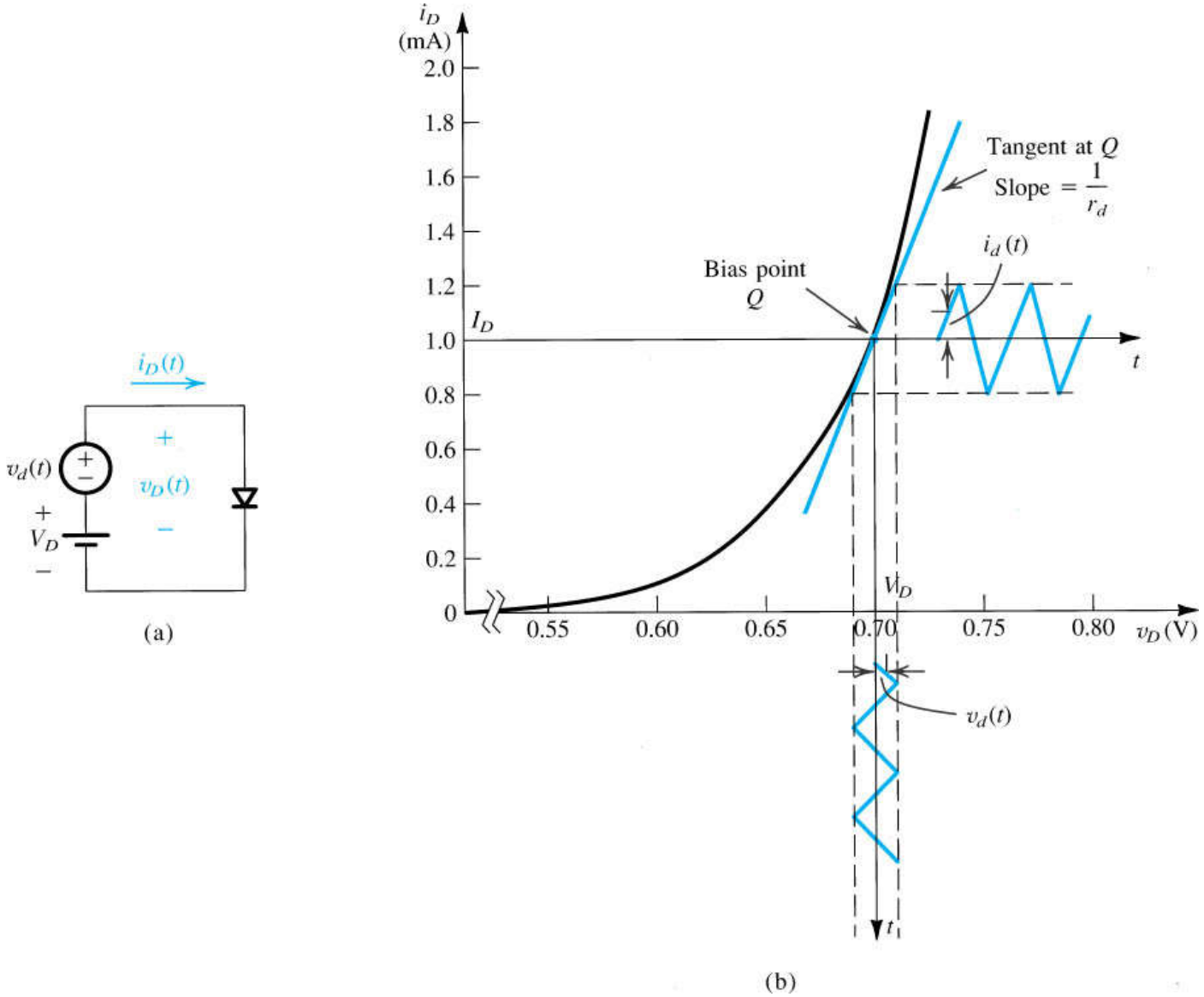


Figure 3.17 Development of the diode small-signal model. Note that the numerical values shown are for a diode with $n = 2$.

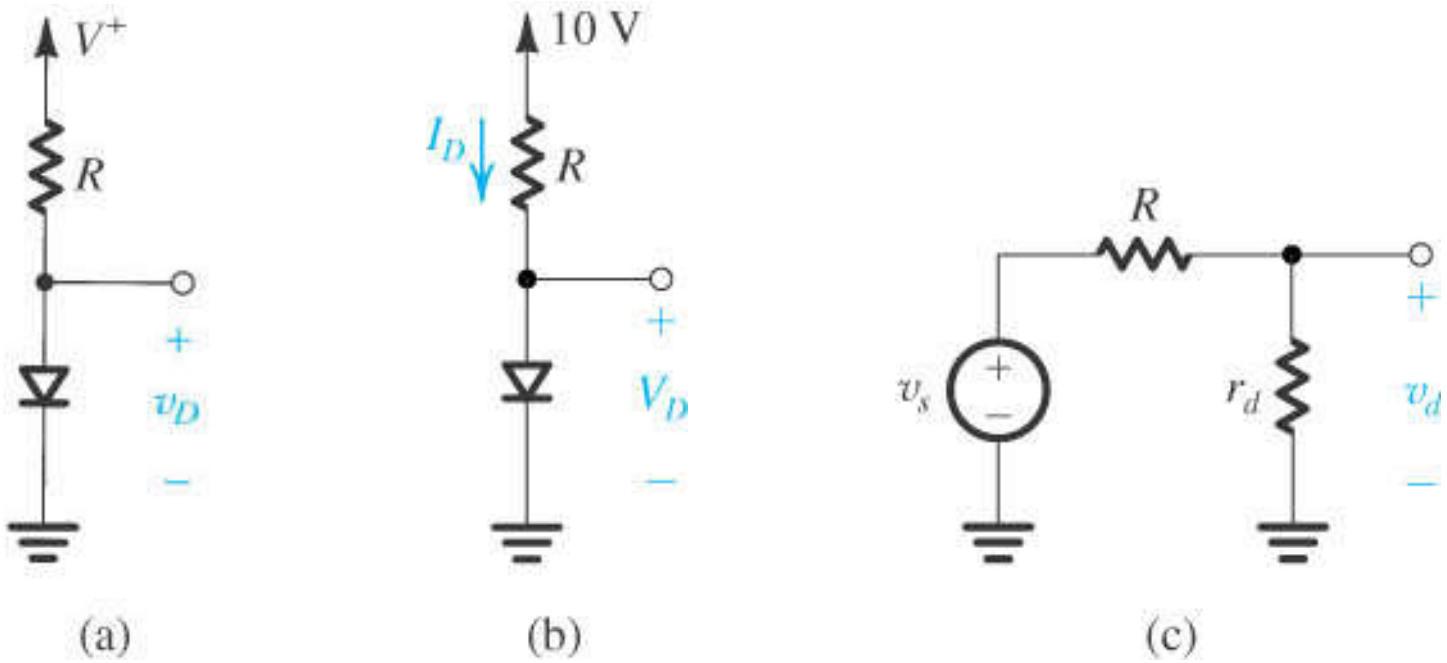


Figure 3.18 **(a)** Circuit for Example 3.6. **(b)** Circuit for calculating the dc operating point. **(c)** Small-signal equivalent circuit.

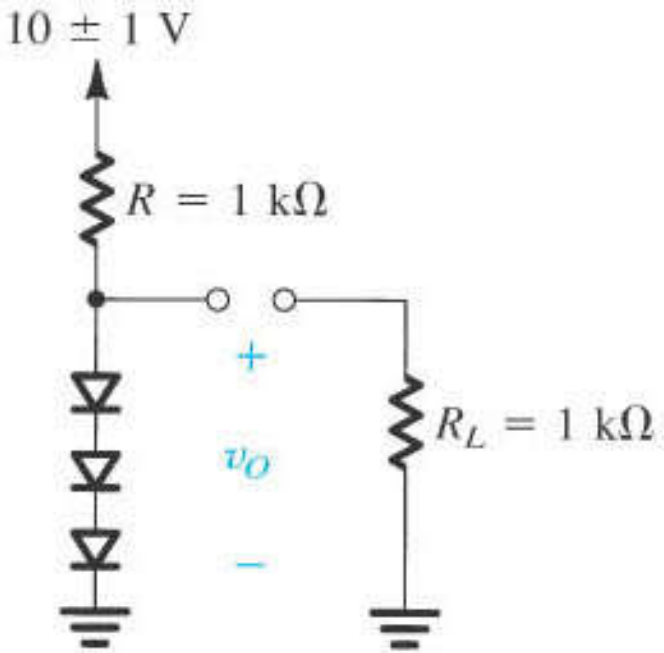


Figure 3.19 Circuit for Example 3.7.

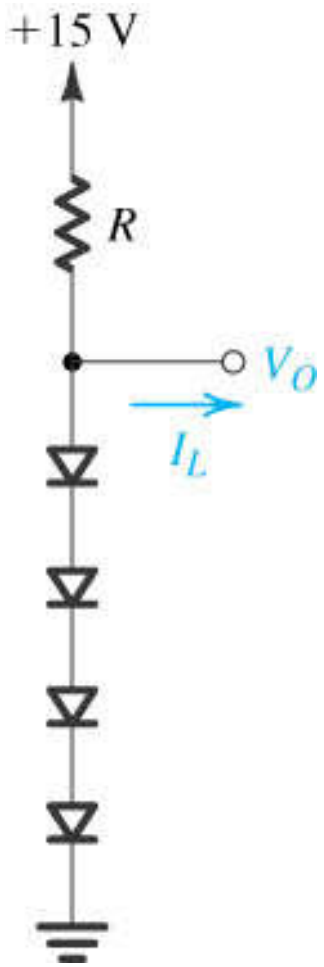


Figure E3.16

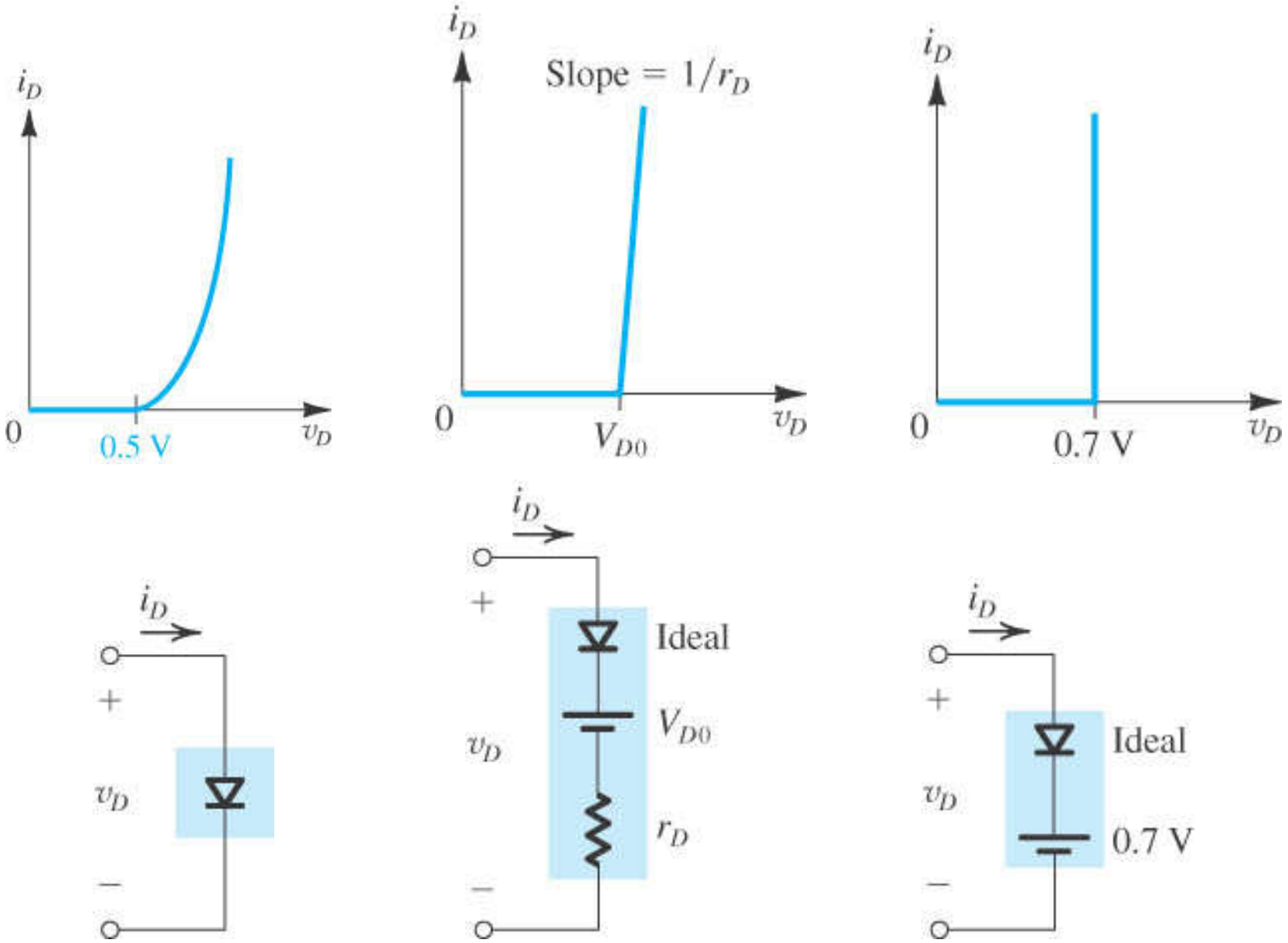


Table 3.1 Modeling the Diode Forward Characteristic

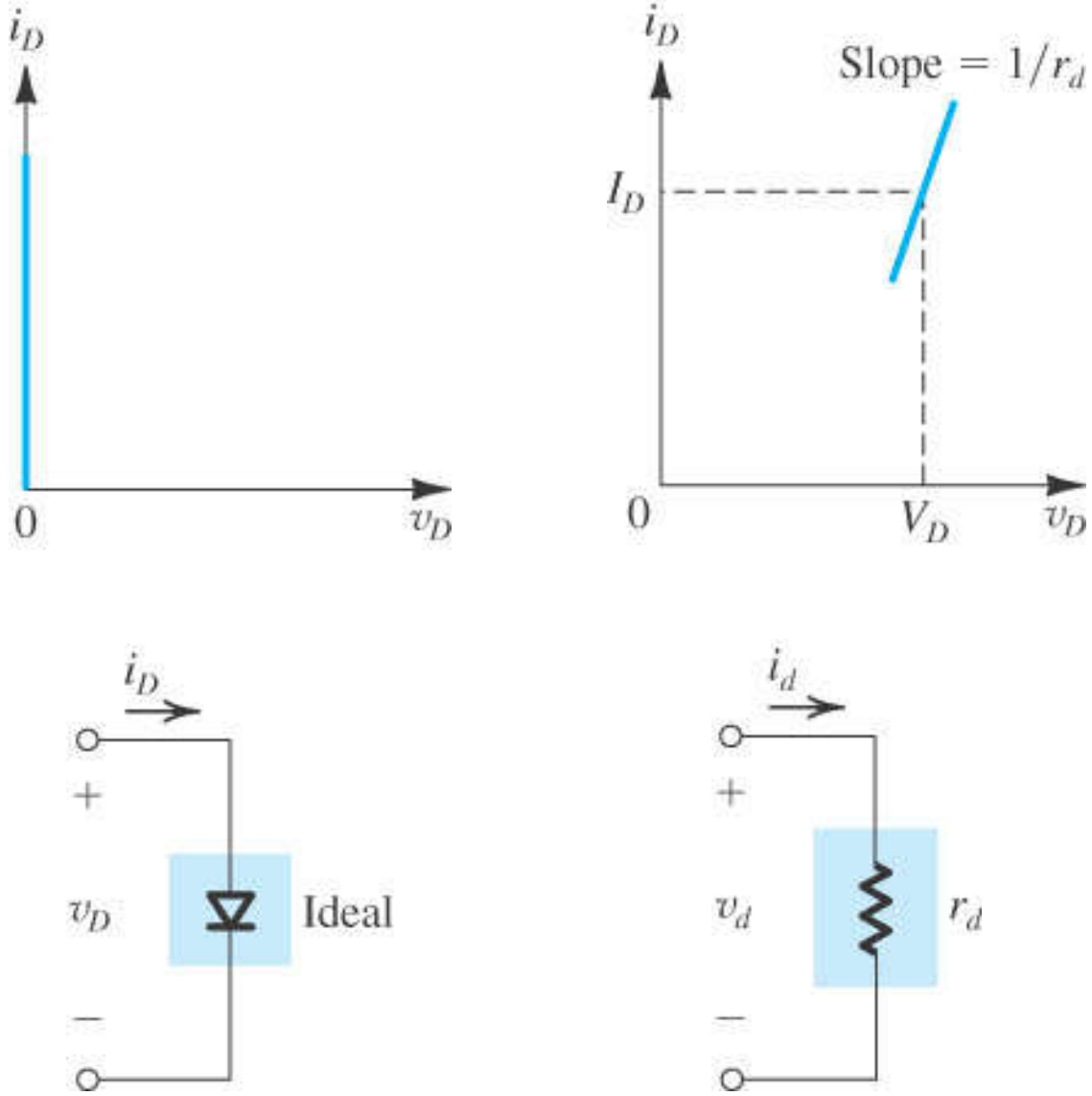


Table 3.1 ***(Continued)***

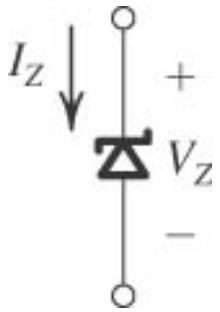


Figure 3.20 Circuit symbol for a zener diode.

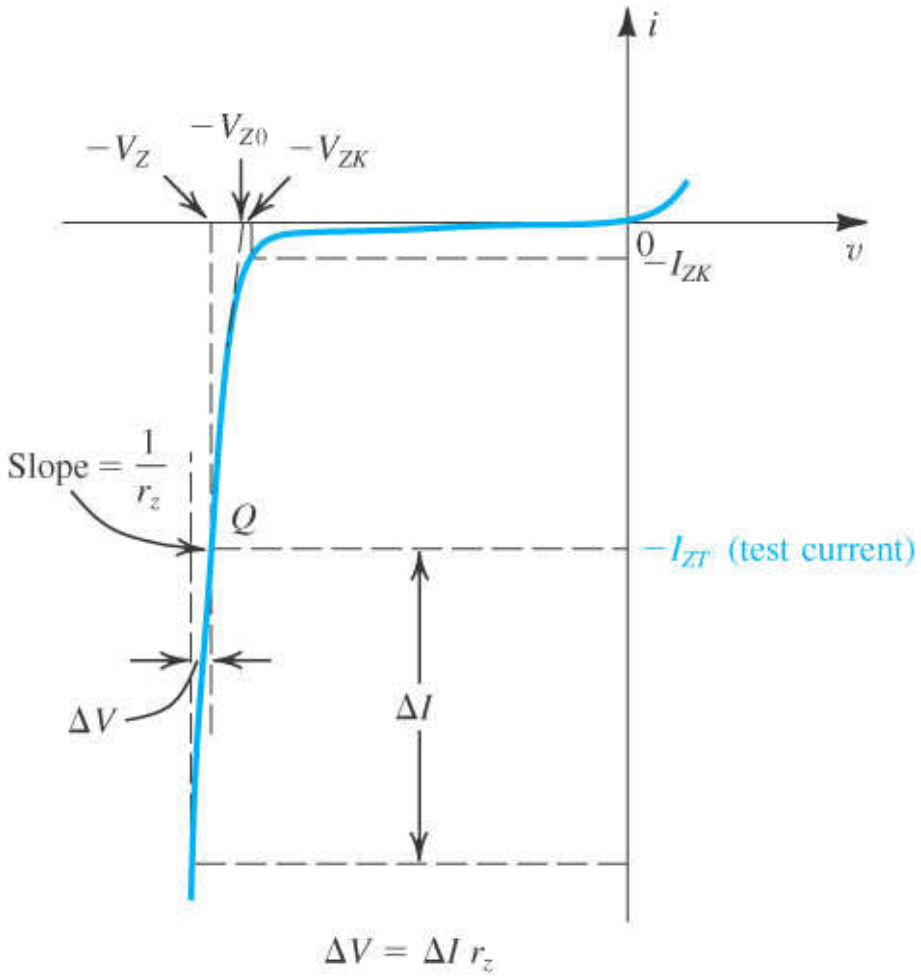


Figure 3.21 The diode *i–v* characteristic with the breakdown region shown in some detail.

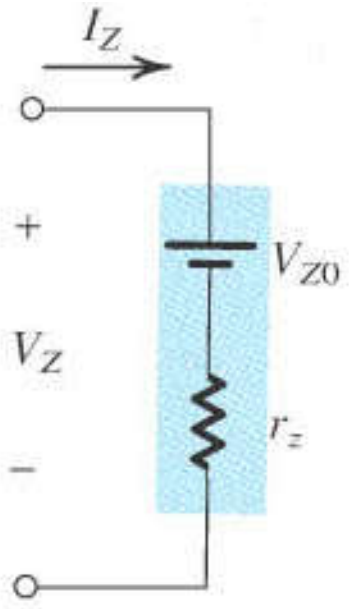


Figure 3.22 Model for the zener diode.

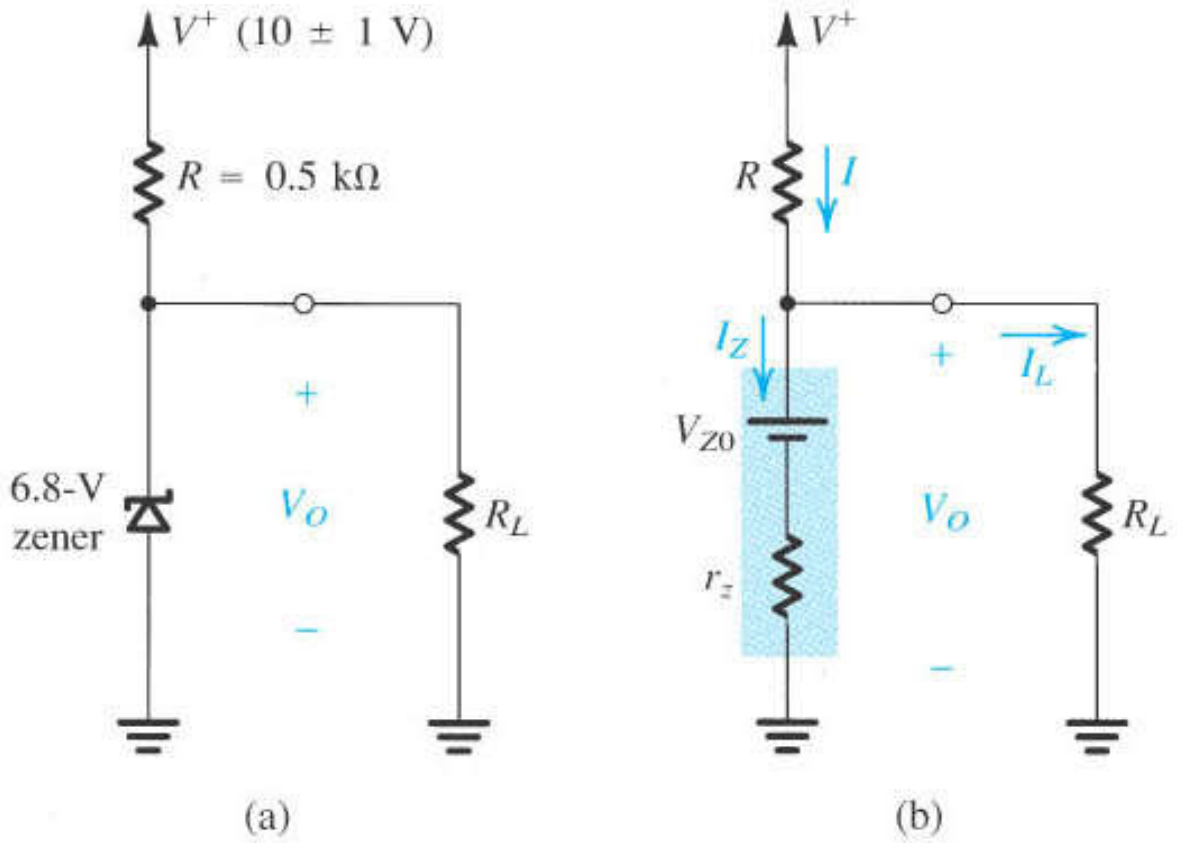


Figure 3.23 **(a)** Circuit for Example 3.8. **(b)** The circuit with the zener diode replaced with its equivalent circuit model.

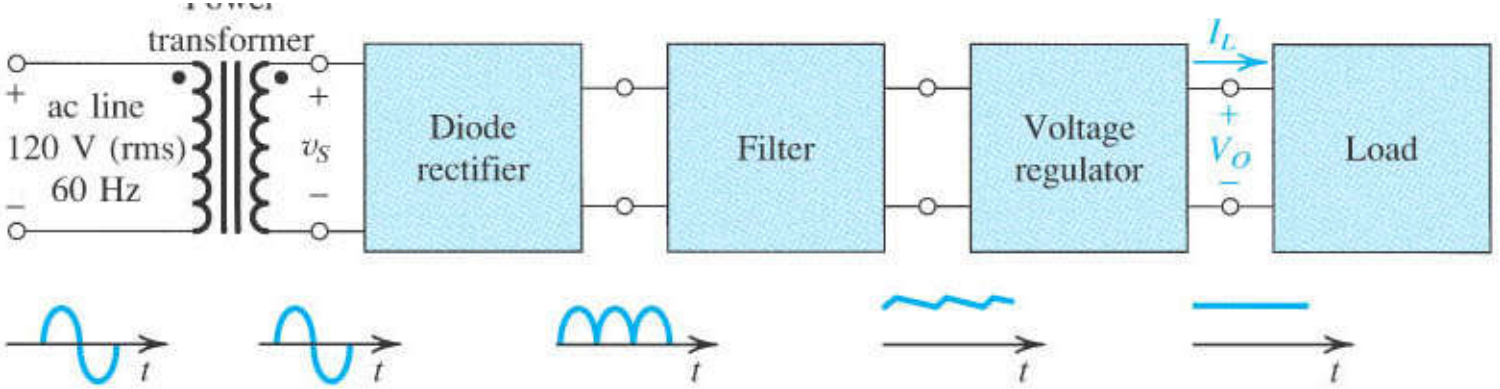


Figure 3.24 Block diagram of a dc power supply.

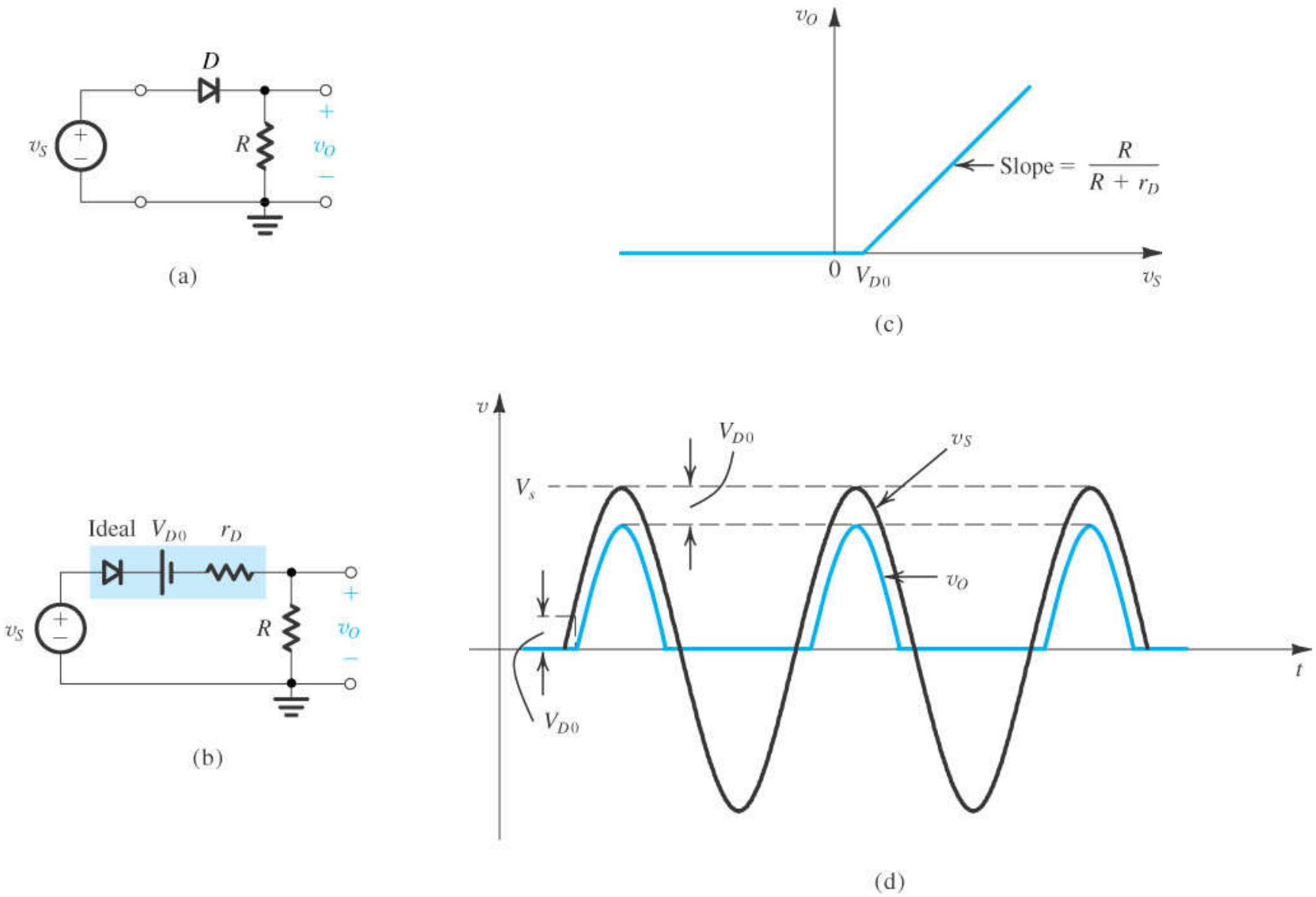


Figure 3.25 **(a)** Half-wave rectifier. **(b)** Equivalent circuit of the half-wave rectifier with the diode replaced with its battery-plus-resistance model. **(c)** Transfer characteristic of the rectifier circuit. **(d)** Input and output waveforms, assuming that r_D ! R.

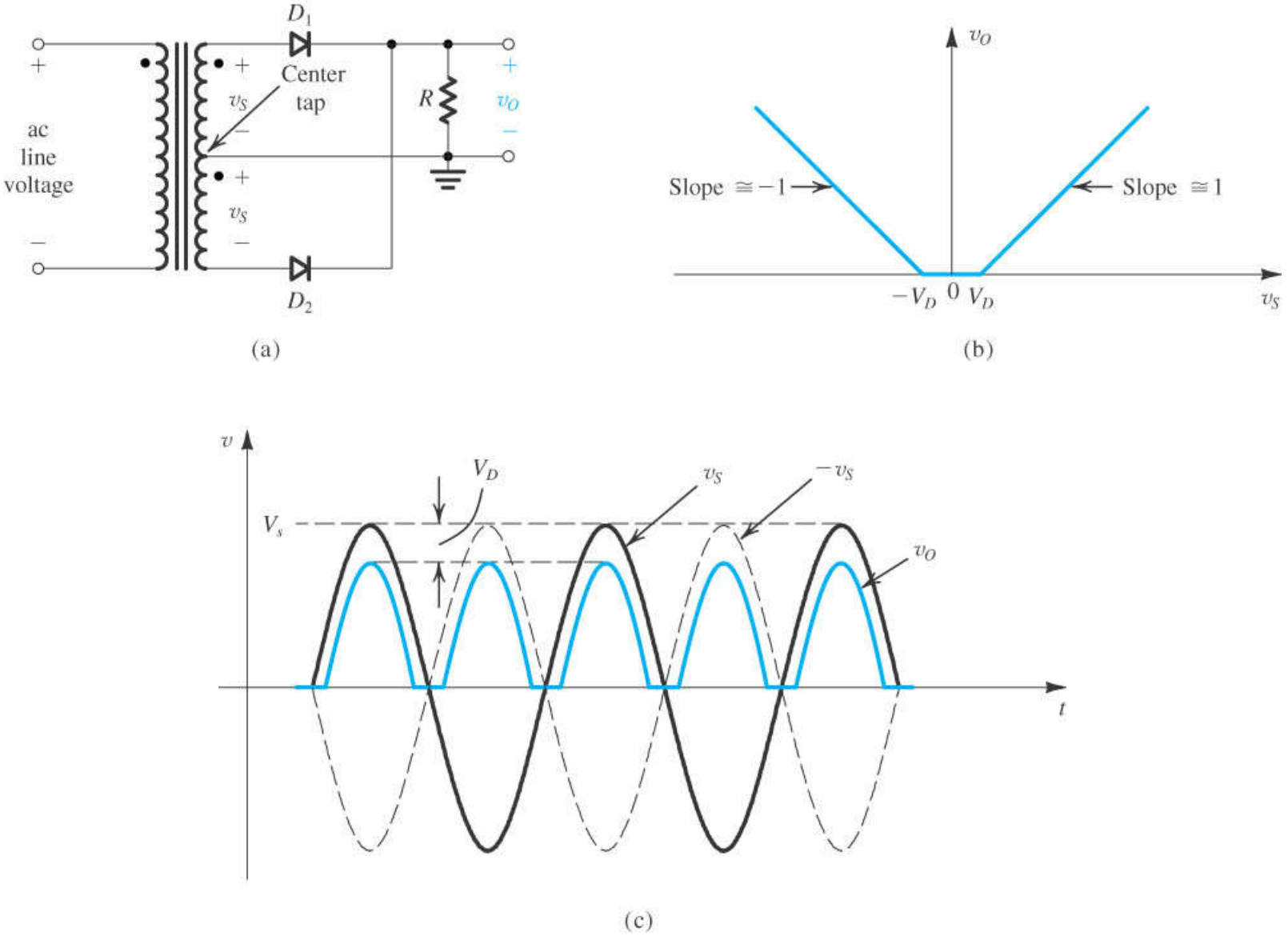


Figure 3.26 Full-wave rectifier utilizing a transformer with a center-tapped secondary winding: **(a)** circuit; **(b)** transfer characteristic assuming a constant-voltage-drop model for the diodes; **(c)** input and output waveforms.

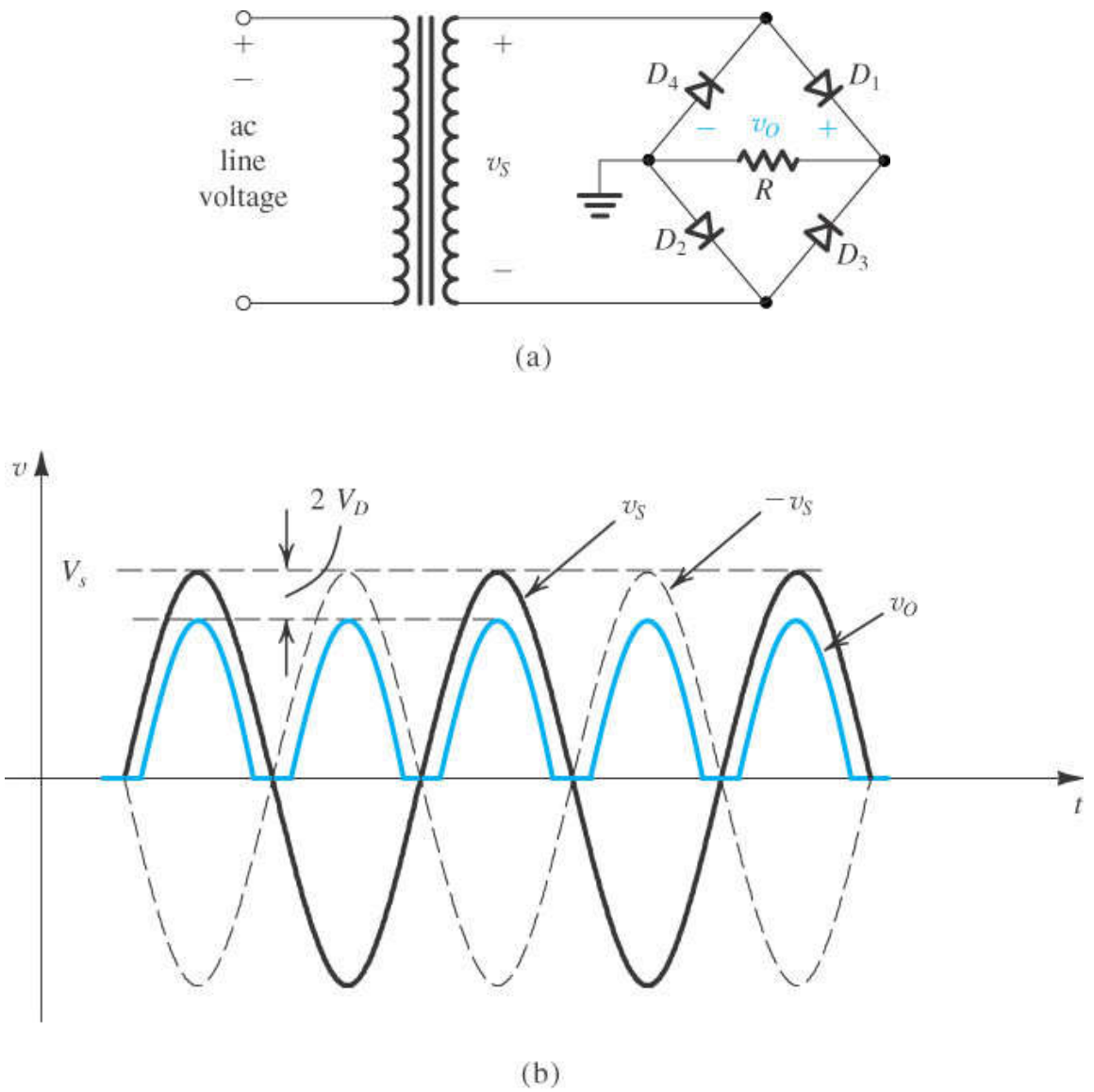


Figure 3.27 The bridge rectifier: **(a)** circuit; **(b)** input and output waveforms.

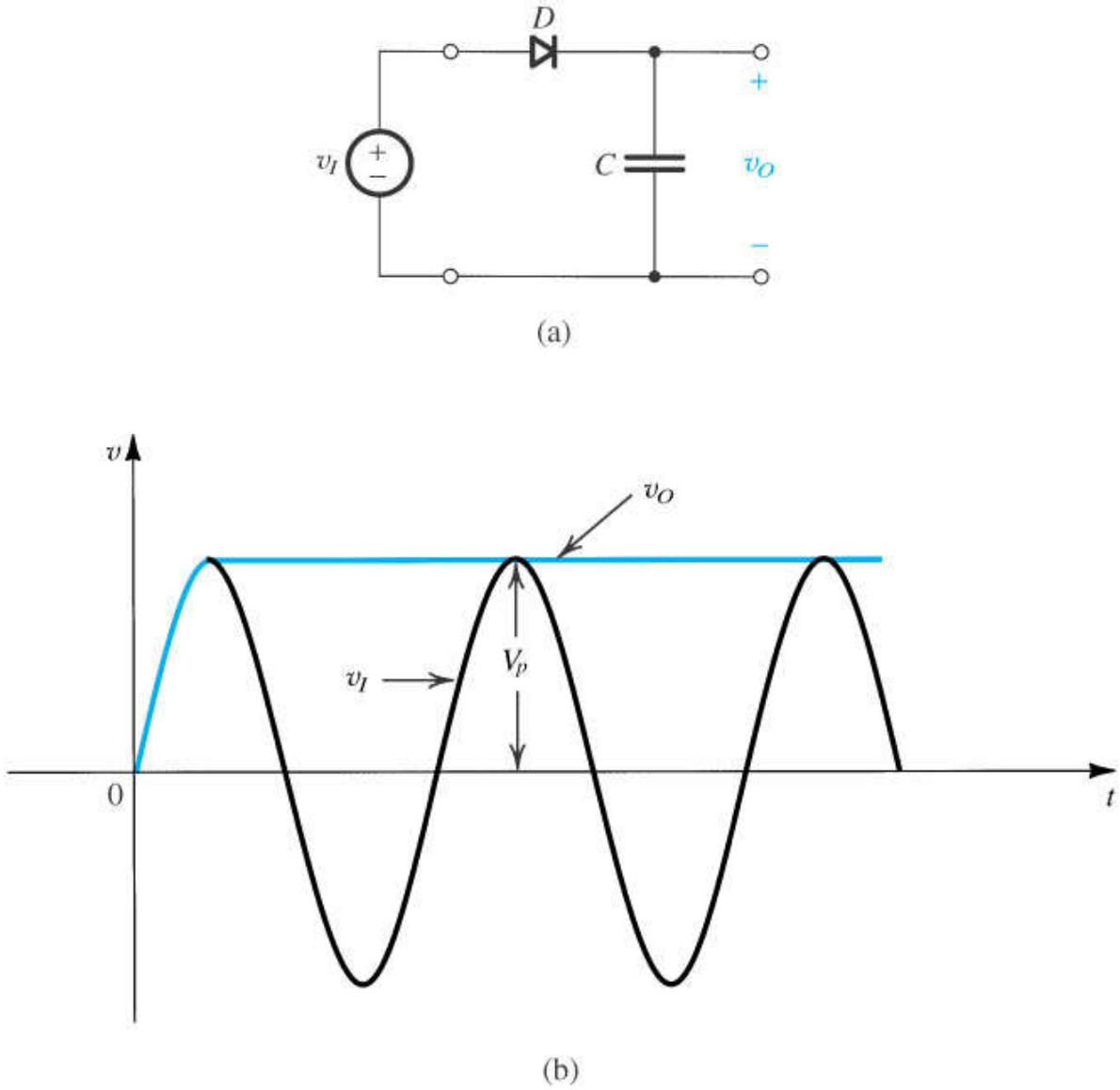


Figure 3.28 **(a)** A simple circuit used to illustrate the effect of a filter capacitor. **(b)** Input and output waveforms assuming an ideal diode. Note that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a peak rectifier or a peak detector.

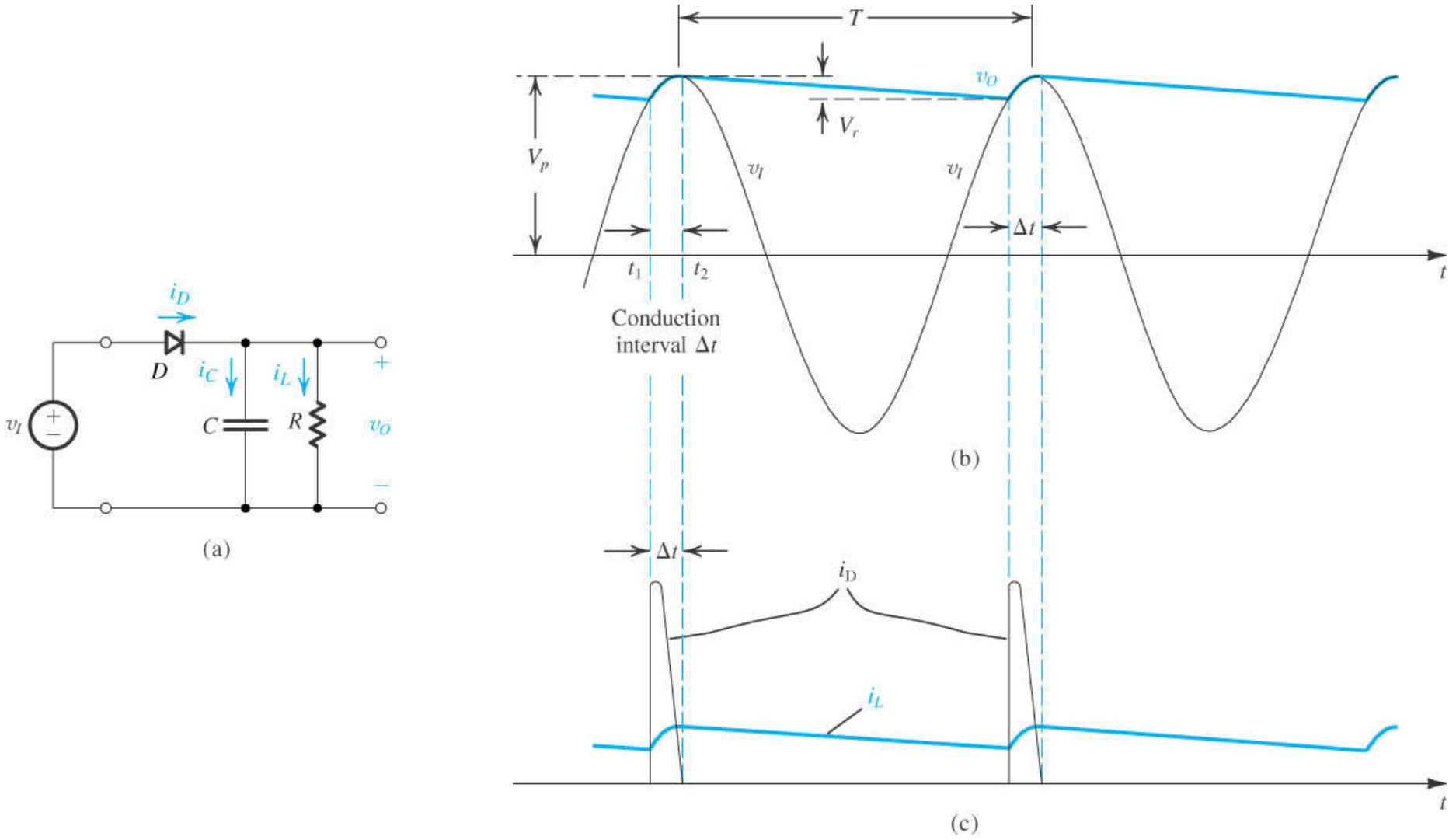


Figure 3.29 Voltage and current waveforms in the peak rectifier circuit with $CR \gg T$. The diode is assumed ideal.

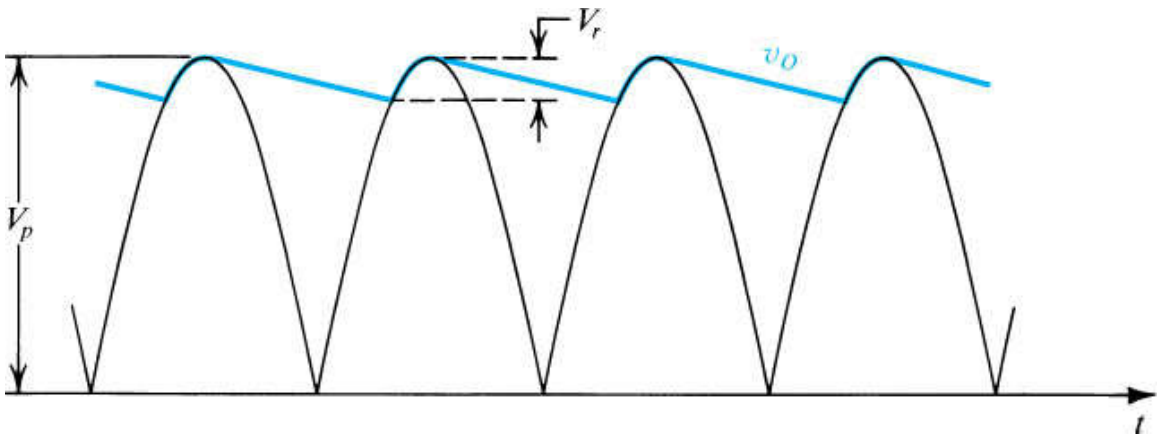


Figure 3.30 Waveforms in the full-wave peak rectifier.

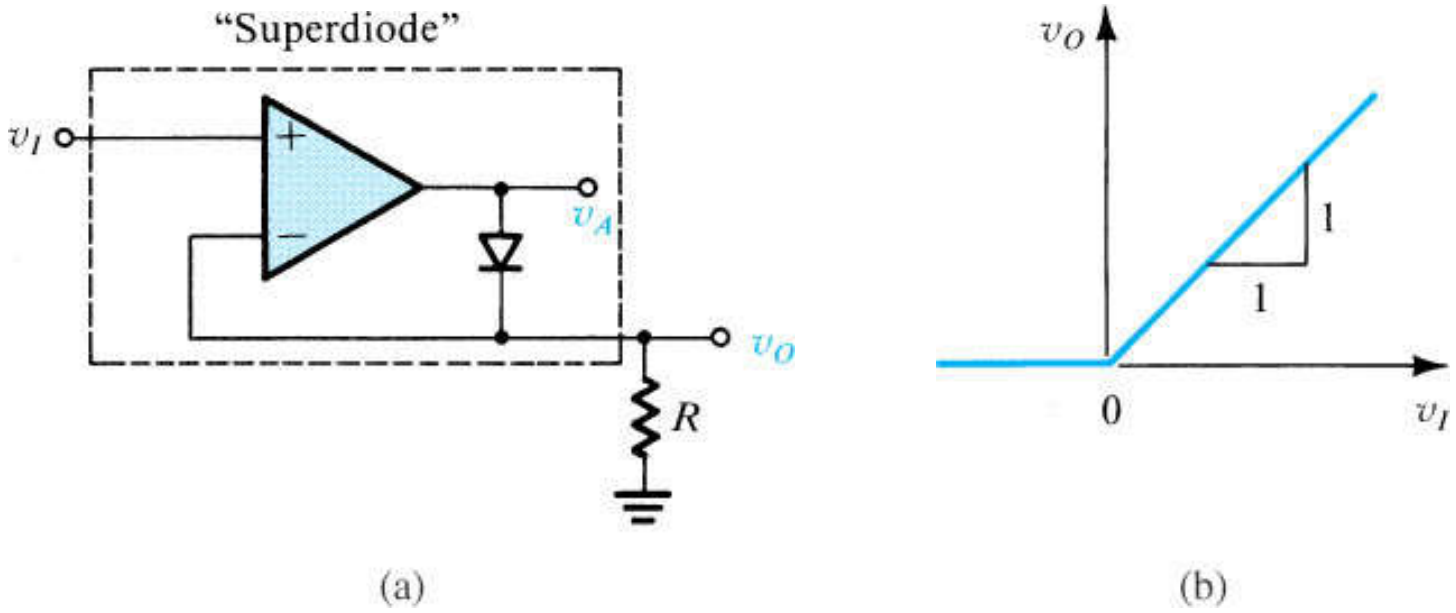


Figure 3.31 The "superdiode" precision half-wave rectifier and its almost-ideal transfer characteristic. Note that when $v_I > 0$ and the diode conducts, the op amp supplies the load current, and the source is conveniently buffered, an added advantage. Not shown are the op-amp power supplies.

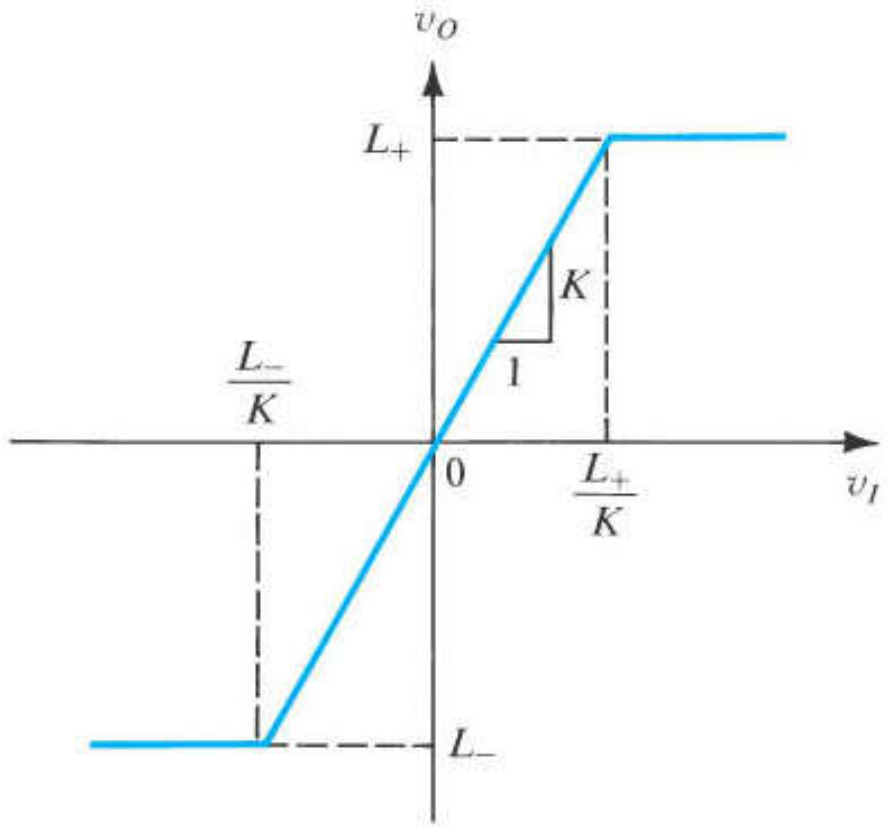


Figure 3.32 General transfer characteristic for a limiter circuit.

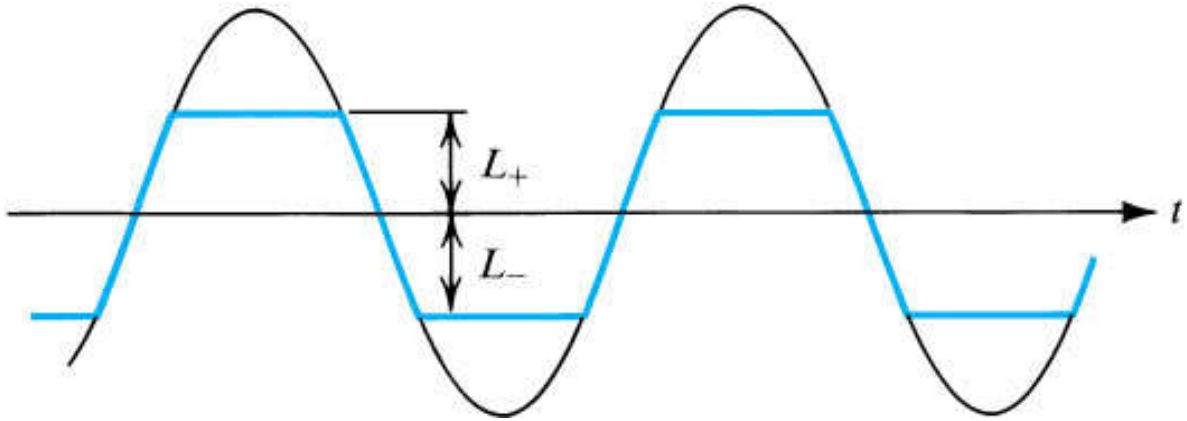


Figure 3.33 Applying a sine wave to a limiter can result in clipping off its two peaks.

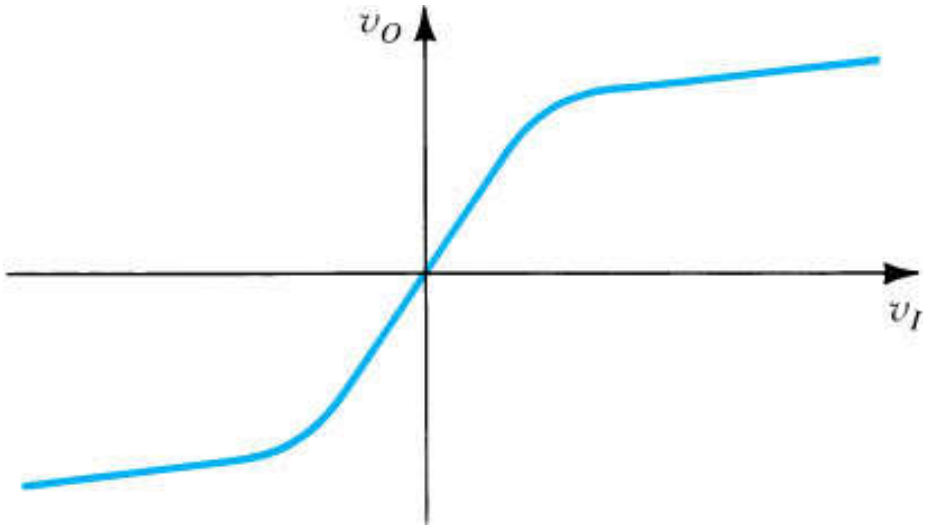


Figure 3.34 Soft limiting.

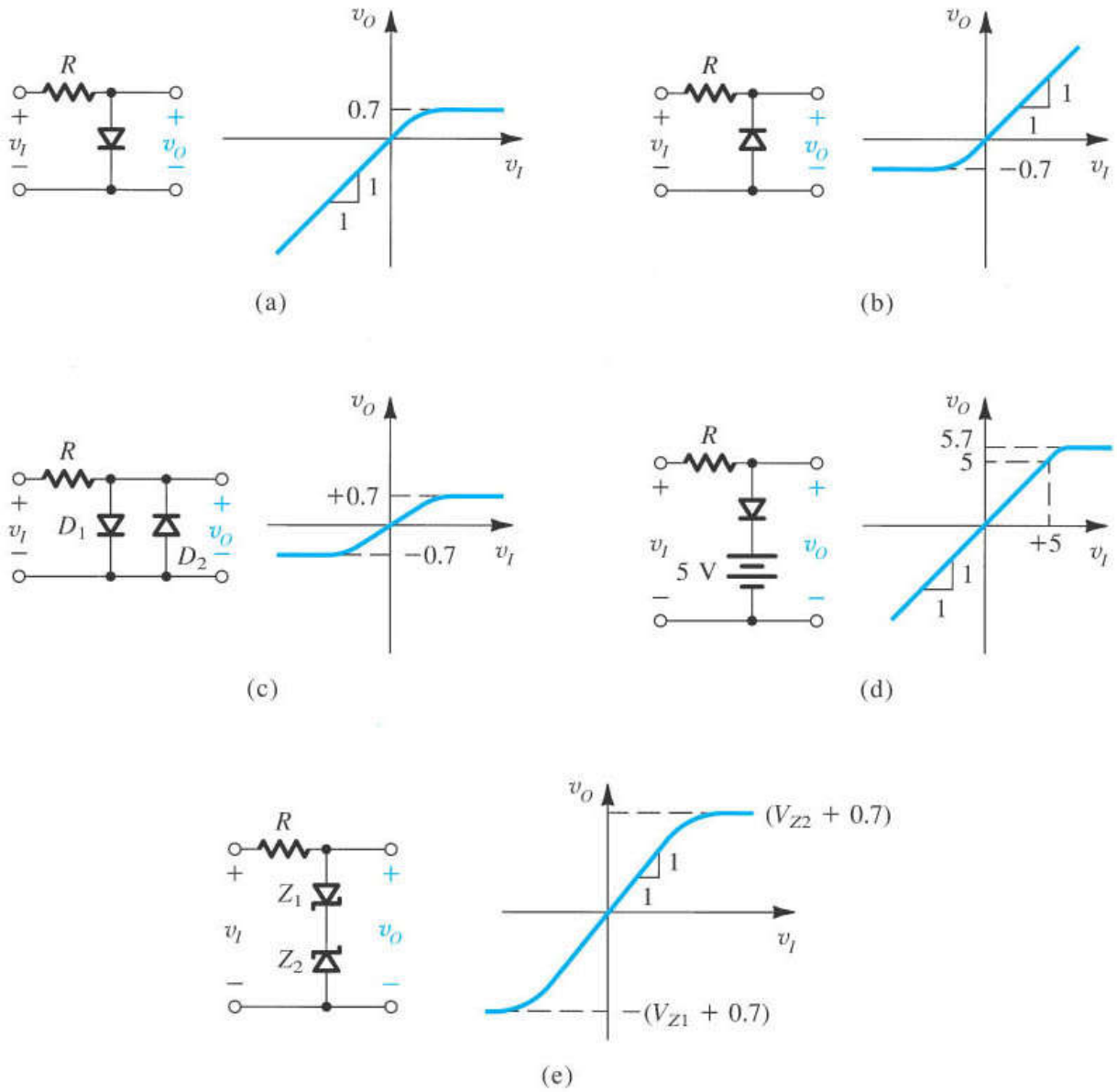


Figure 3.35 A variety of basic limiting circuits.

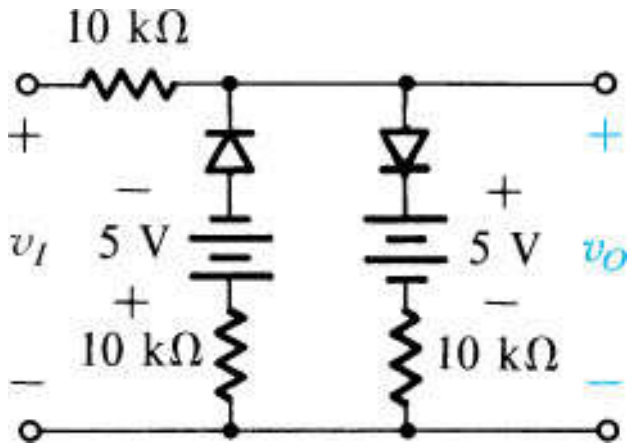


Figure E3.27

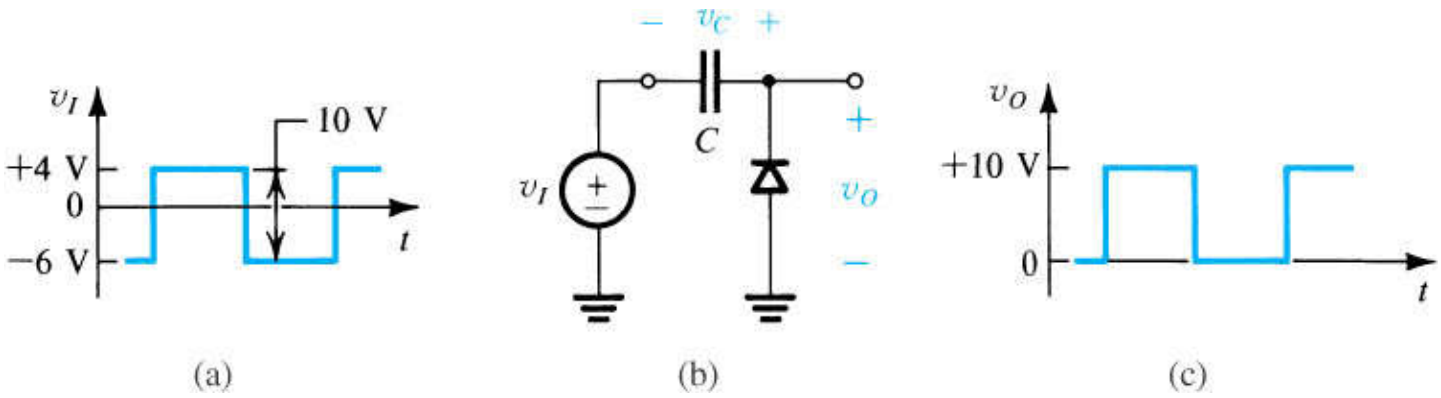


Figure 3.36 The clamped capacitor or dc restorer with a square-wave input and no load.

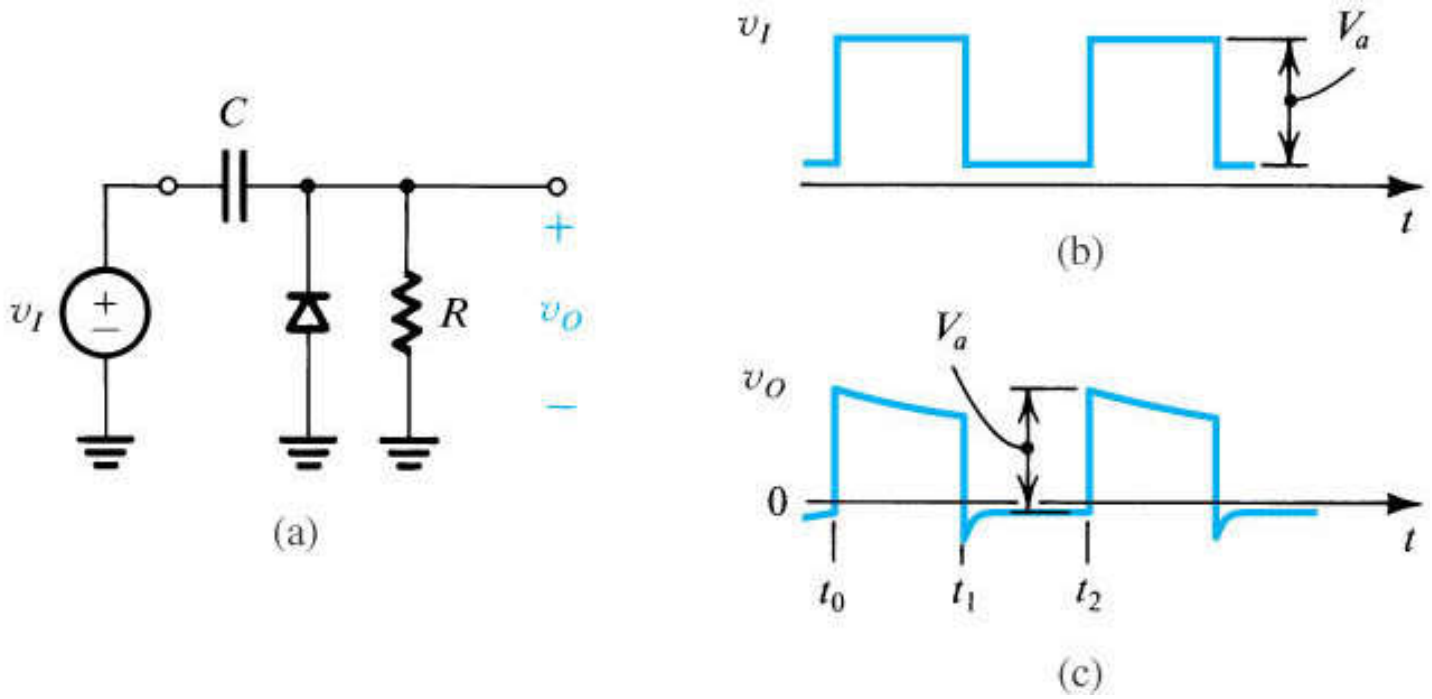
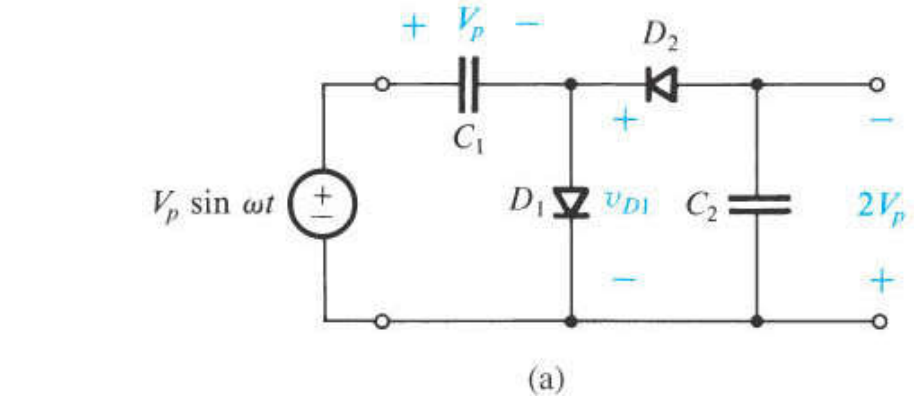
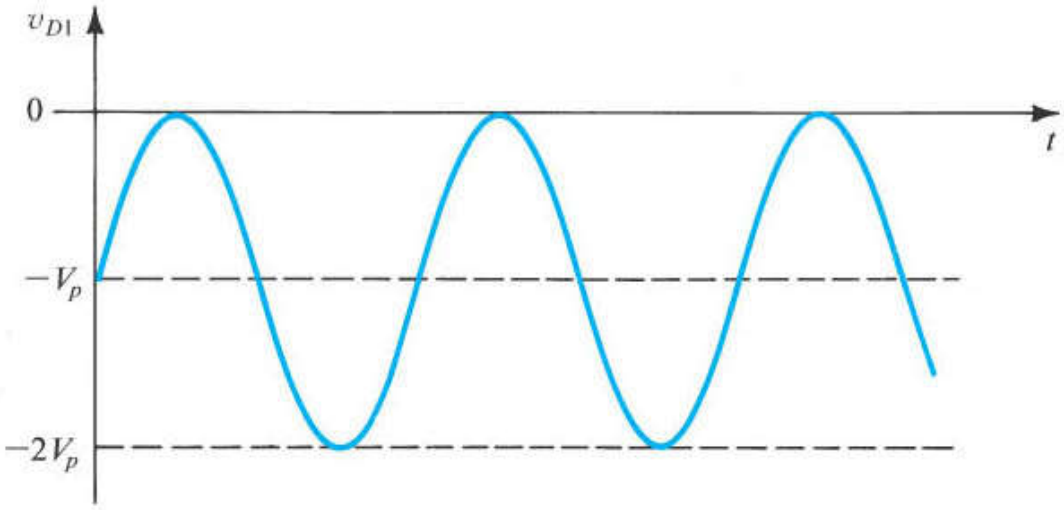


Figure 3.37 The clamped capacitor with a load resistance *R*.



(a)



(b)

Figure 3.38 Voltage doubler: **(a)** circuit; **(b)** waveform of the voltage across D_1.

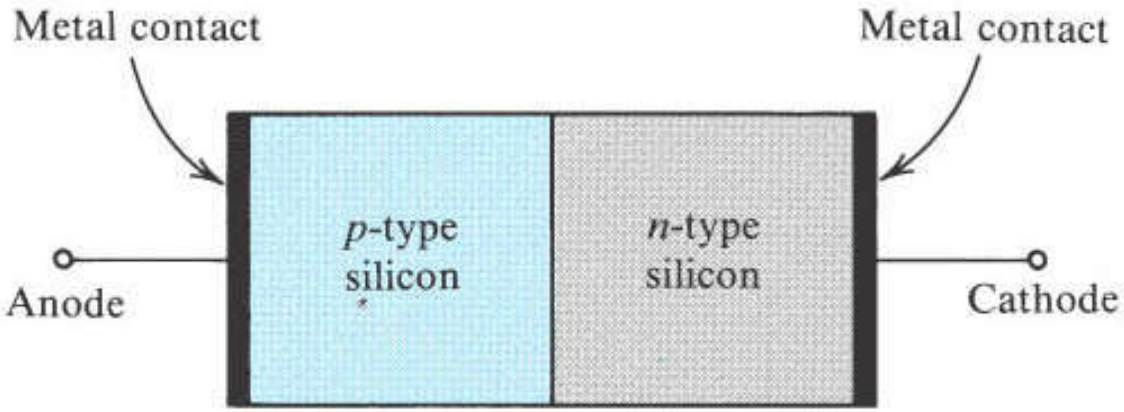


Figure 3.39 Simplified physical structure of the junction diode. (Actual geometries are given in Appendix A.)

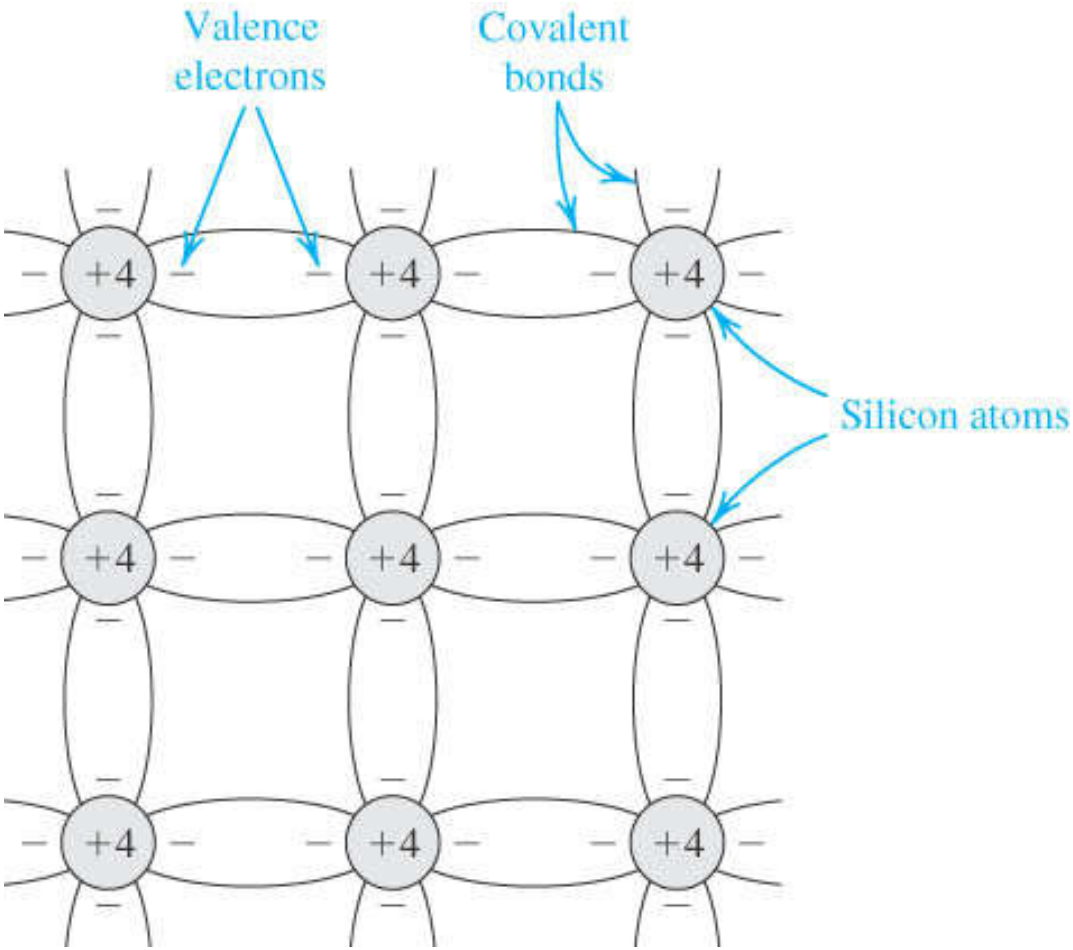


Figure 3.40 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of +4q, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0 K, all bonds are intact and no free electrons are available for current conduction.

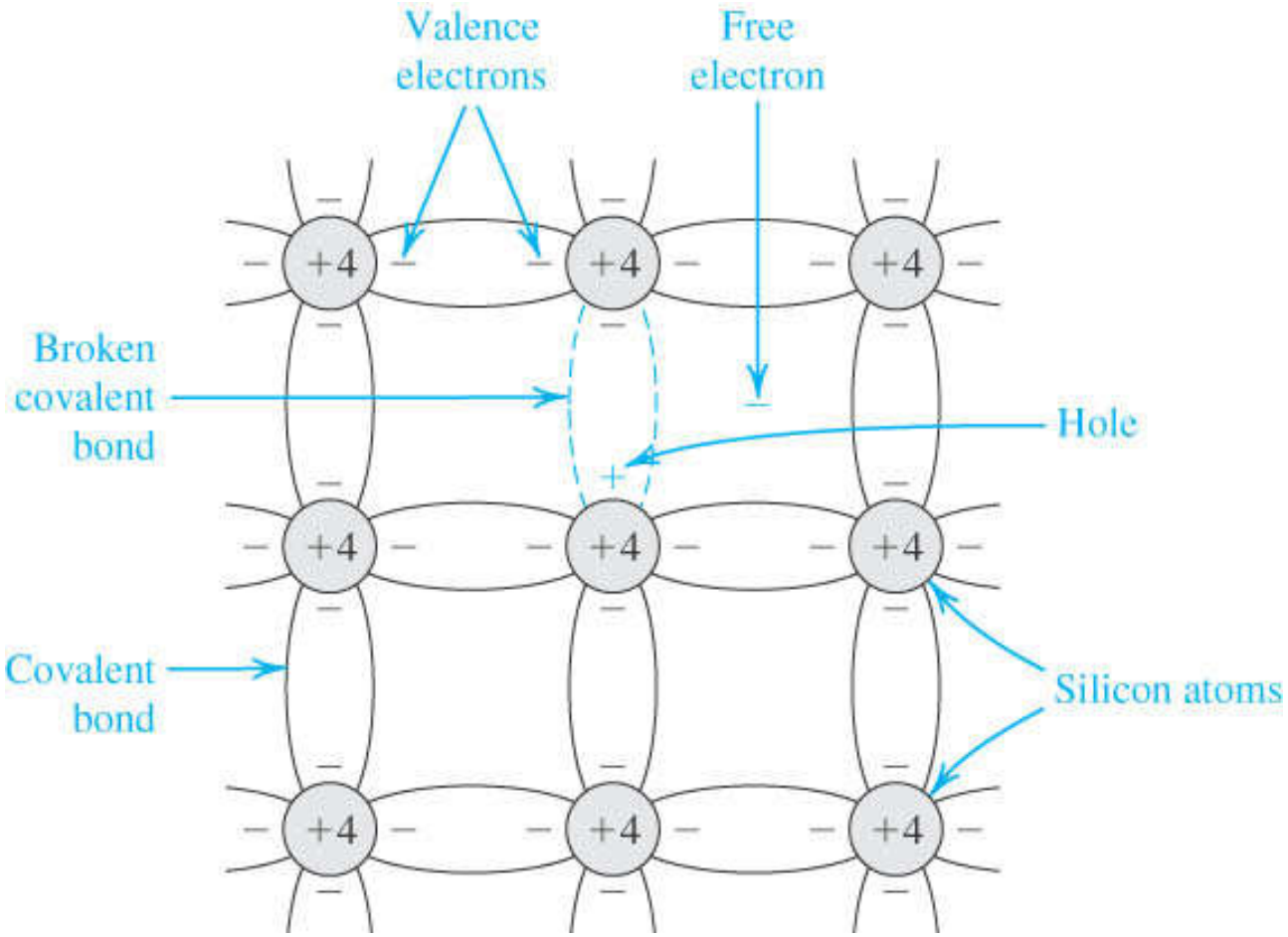


Figure 3.41 At room temperature, some of the covalent bonds are broken by thermal ionization. Each broken bond gives rise to a free electron and a hole, both of which become available for current conduction.

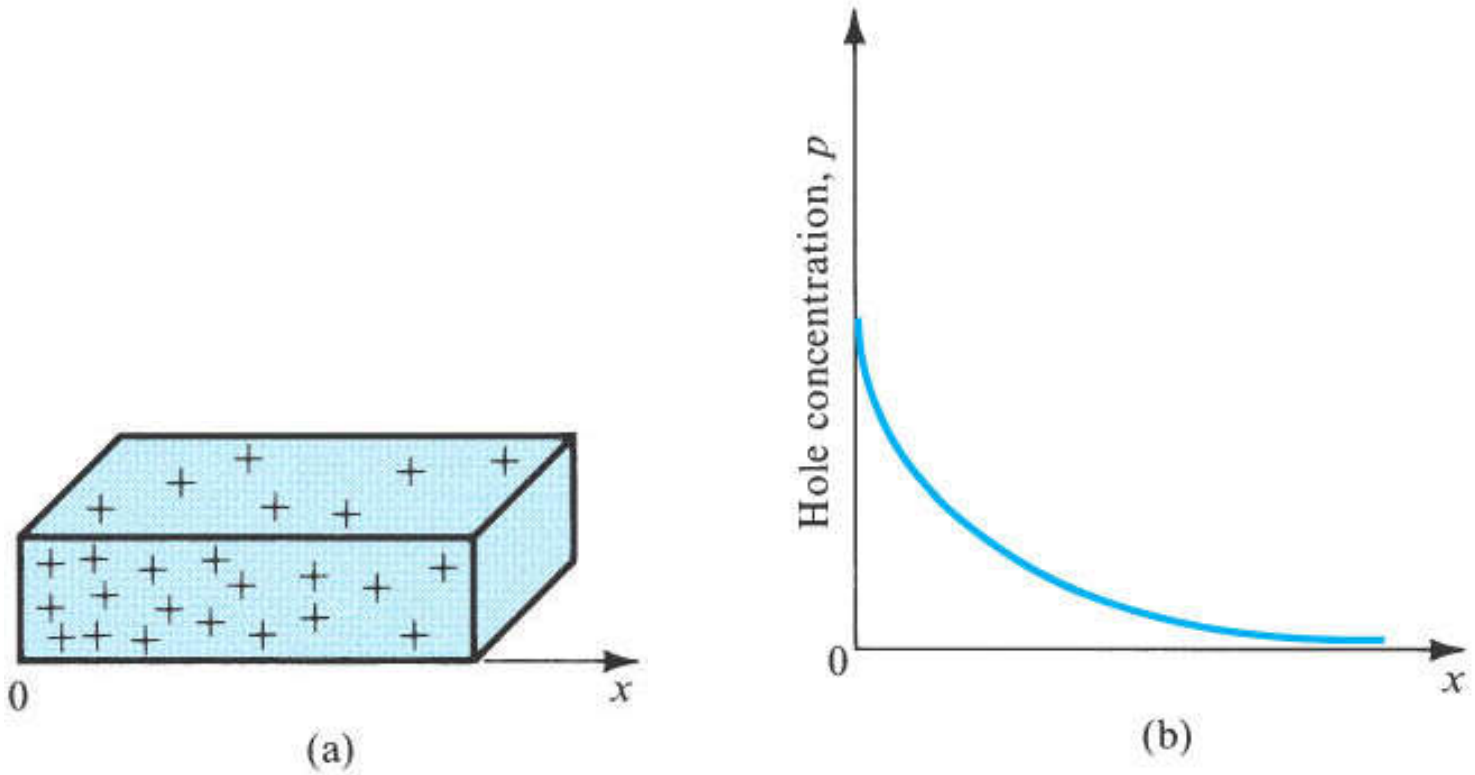


Figure 3.42 A bar of intrinsic silicon **(a)** in which the hole concentration profile shown in **(b)** has been created along the x-axis by some unspecified mechanism.

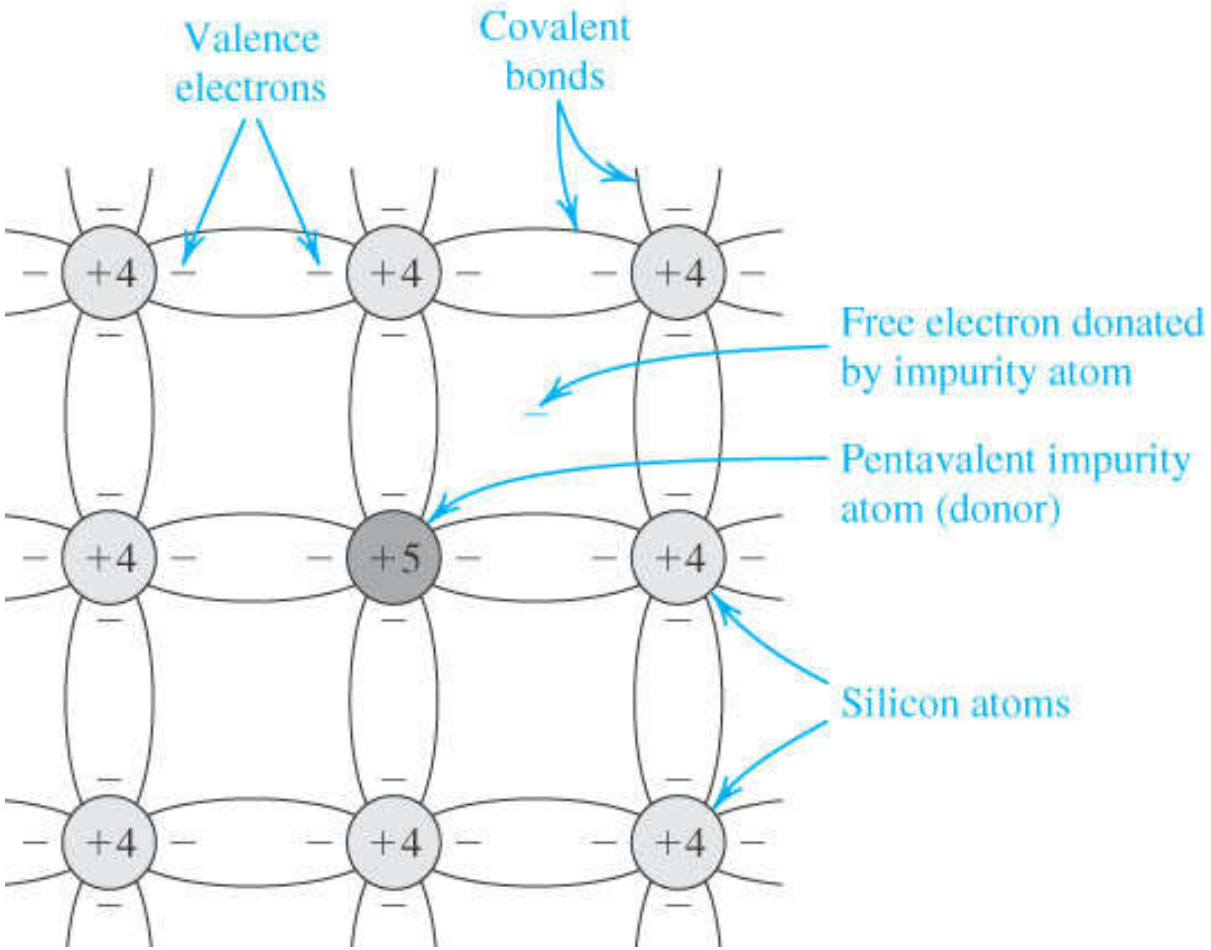


Figure 3.43 A silicon crystal doped by a pentavalent element. Each dopant atom donates a free electron and is thus called a donor. The doped semiconductor becomes *n* type.

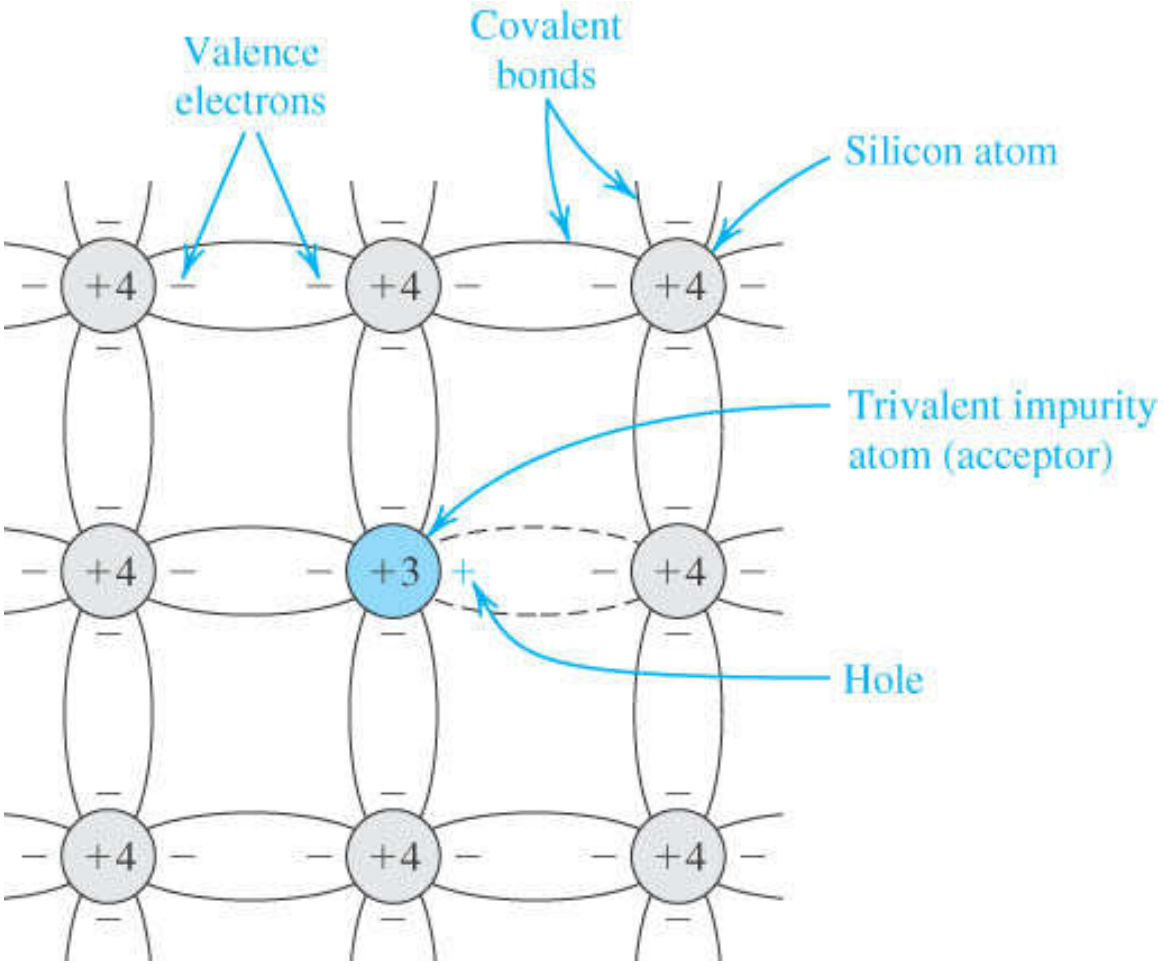


Figure 3.44 A silicon crystal doped with a trivalent impurity. Each dopant atom gives rise to a hole, and the semiconductor becomes *p* type.

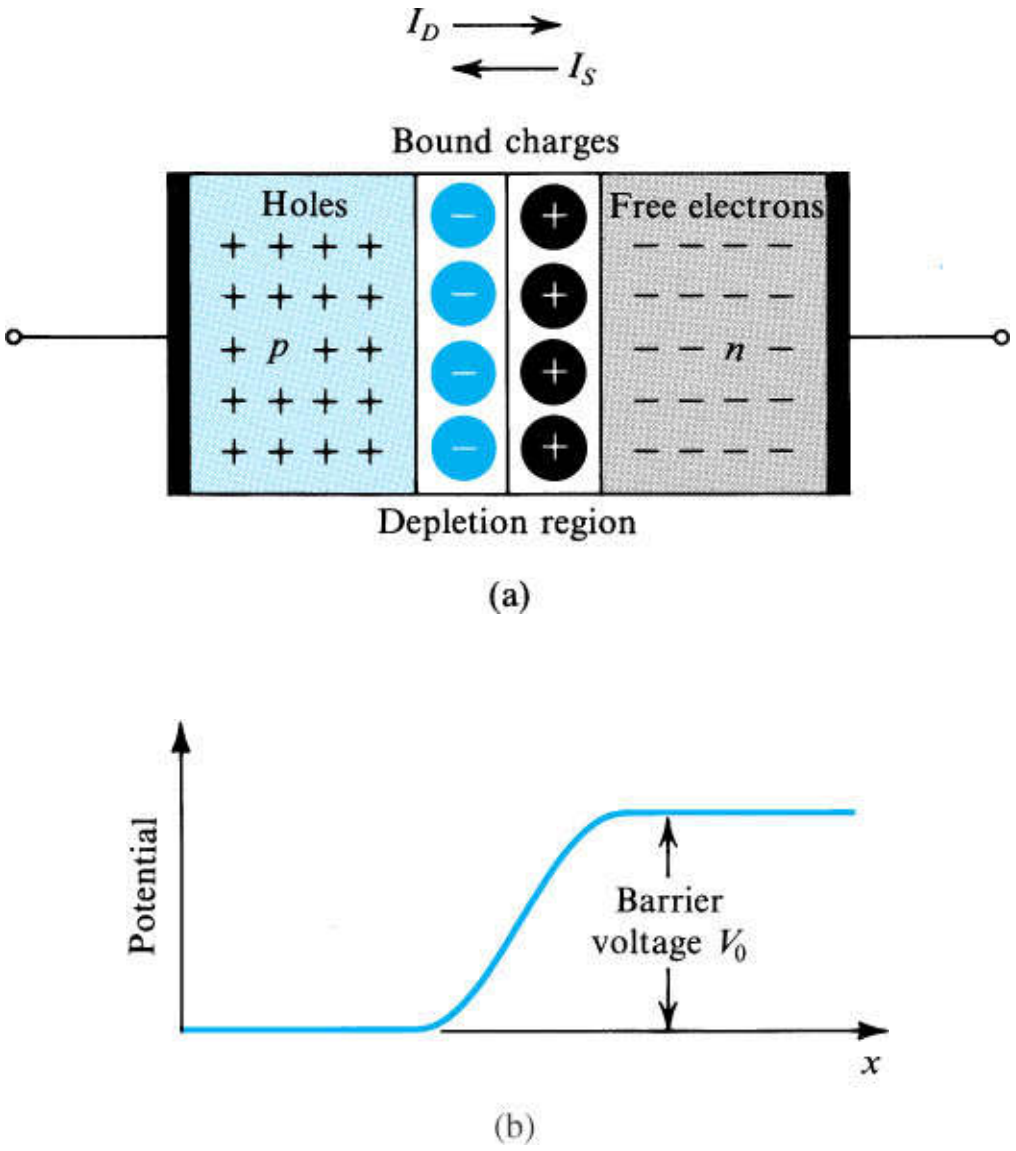


Figure 3.45 **(a)** The *pn* junction with no applied voltage (open-circuited terminals). **(b)** The potential distribution along an axis perpendicular to the junction.

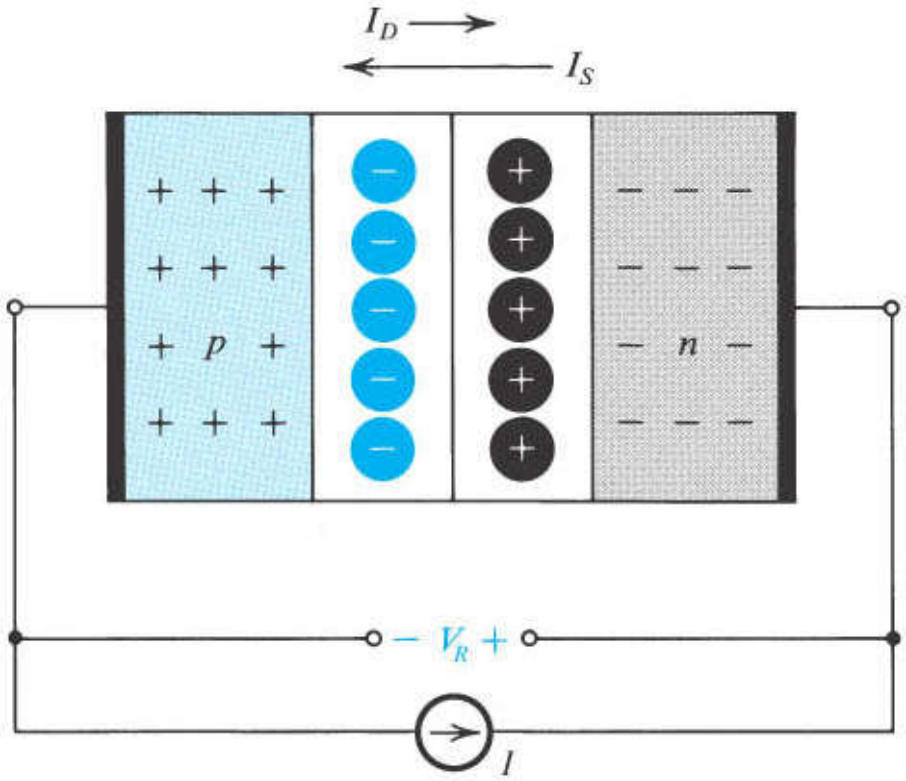


Figure 3.46 The *pn* junction excited by a constant-current source I in the reverse direction. To avoid breakdown, I is kept smaller than I_S. Note that the depletion layer widens and the barrier voltage increases by V_R volts, which appears between the terminals as a reverse voltage.

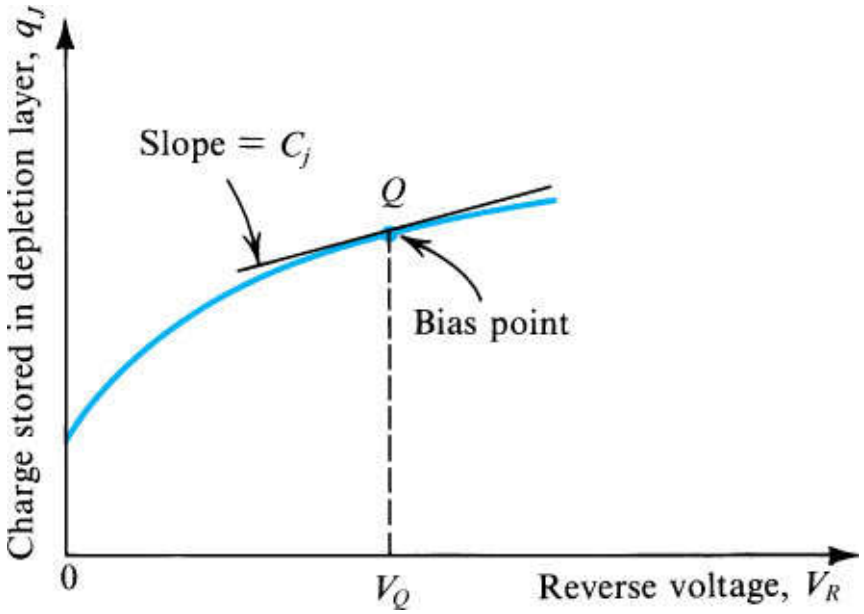


Figure 3.47 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R.

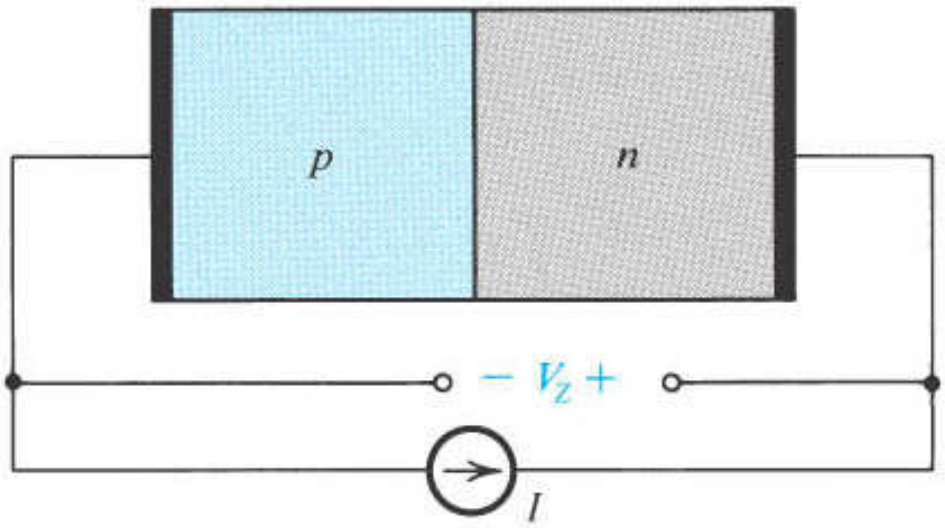


Figure 3.48 The *pn* junction excited by a reverse-current source I, where $I > I_S$. The junction breaks down, and a voltage V_Z, with the polarity indicated, develops across the junction.

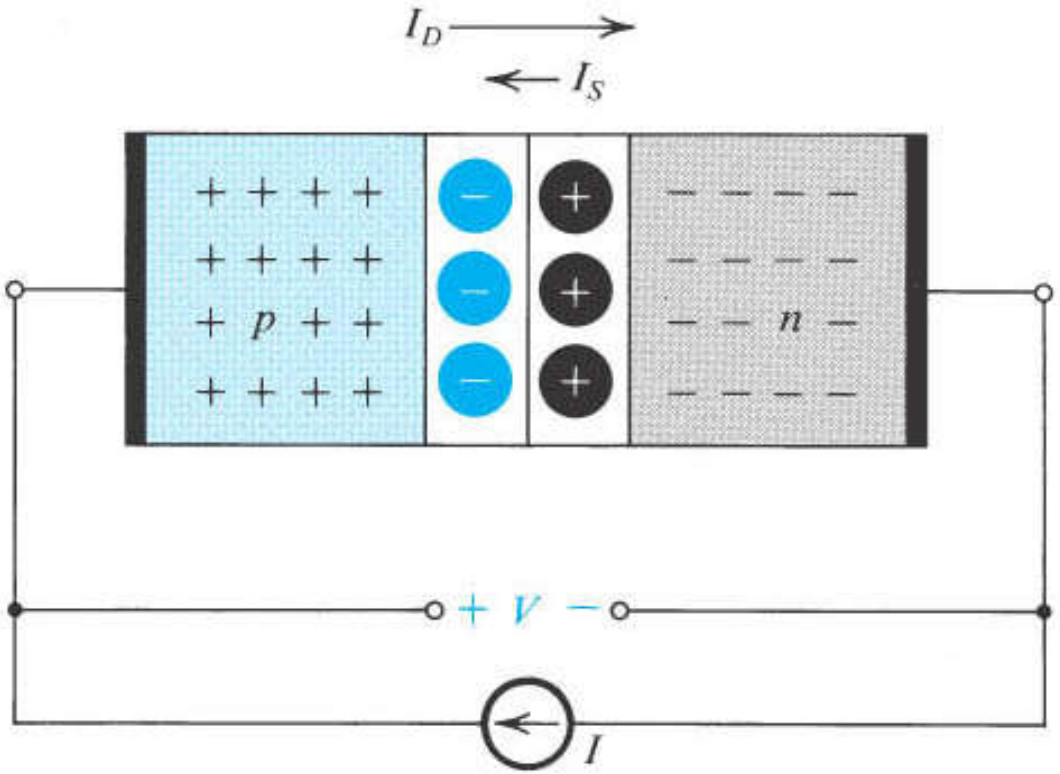


Figure 3.49 The *pn* junction excited by a constant-current source supplying a current I in the forward direction. The depletion layer narrows and the barrier voltage decreases by V volts, which appears as an external voltage in the forward direction.

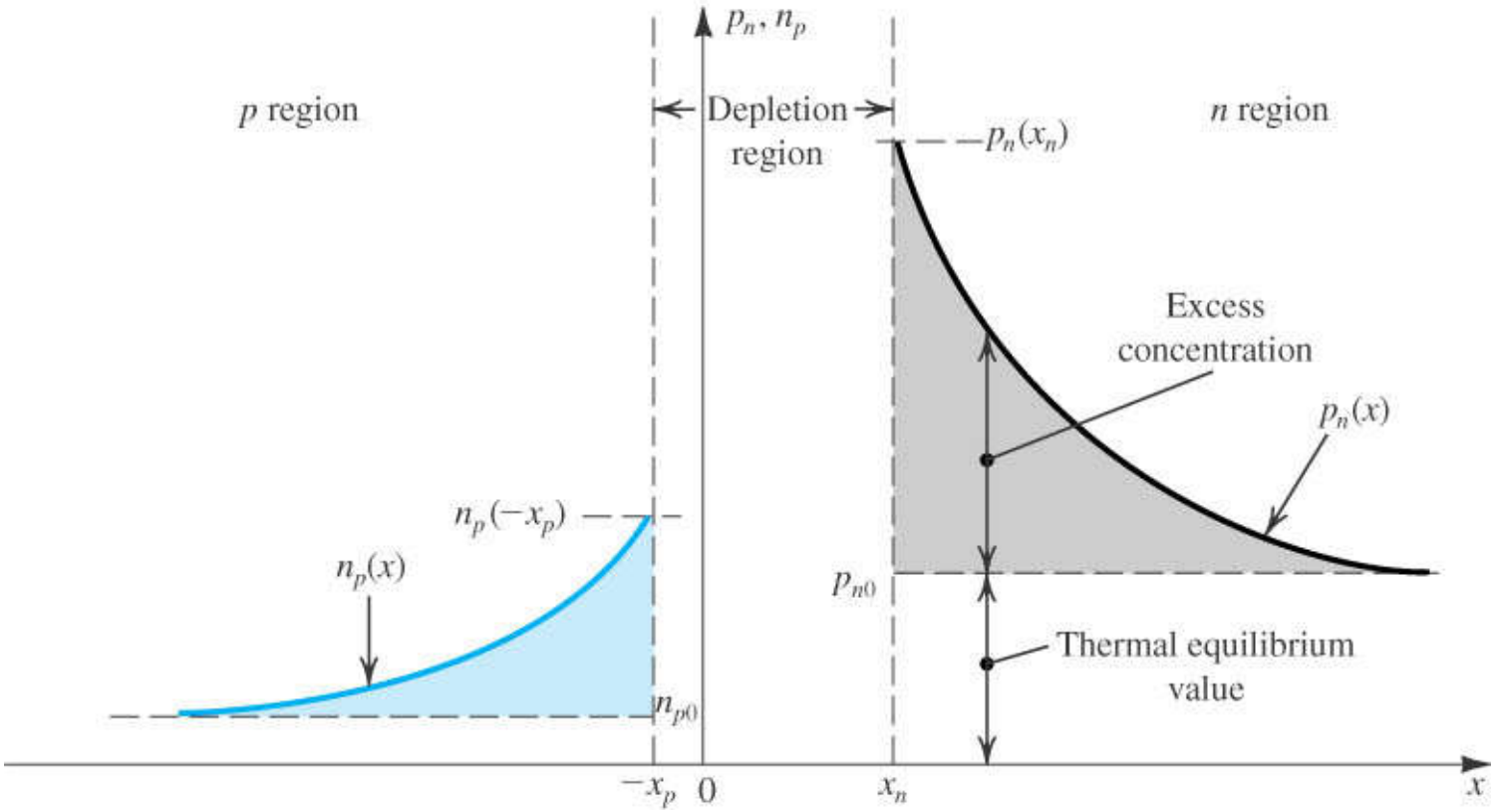
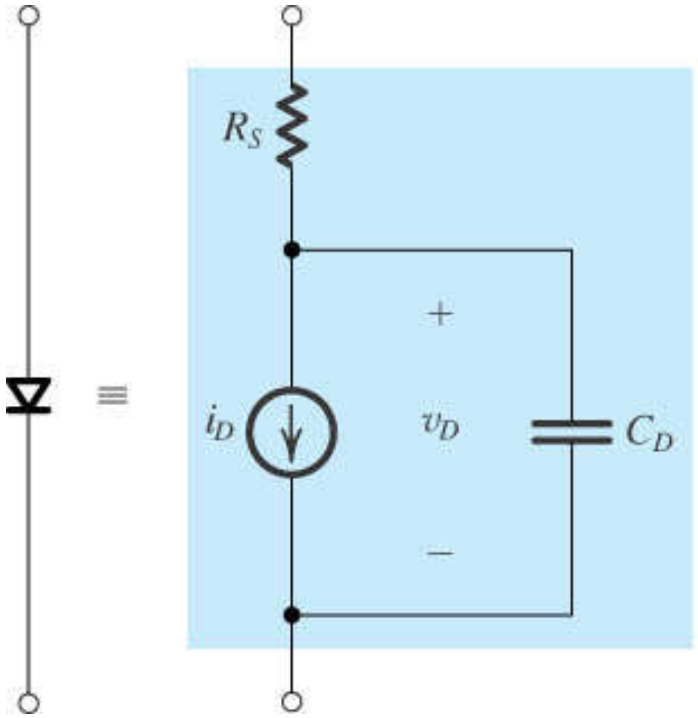


Figure 3.50 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; N_A @ N_D.



$$i_D = I_S\left(e^{v_D/nV_T} - 1\right)$$

$$C_D = C_d + C_j = \frac{\tau_T}{V_T} I_S e^{v_D/nV_T} + C_{j0}\Big/\left(1 - \frac{v_D}{V_0}\right)^m$$

Figure 3.51 The SPICE diode model.

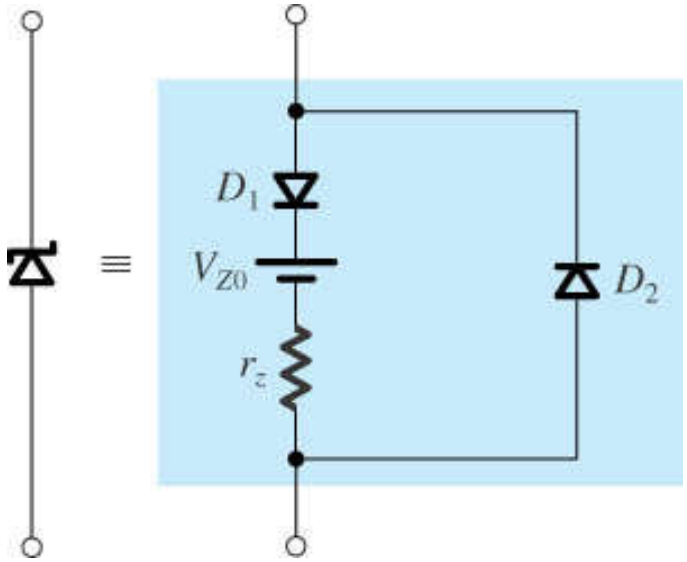


Figure 3.52 Equivalent-circuit model used to simulate the zener diode in SPICE. Diode D_1 is ideal and can be approximated in SPICE by using a very small value for n (say $n = 0.01$).

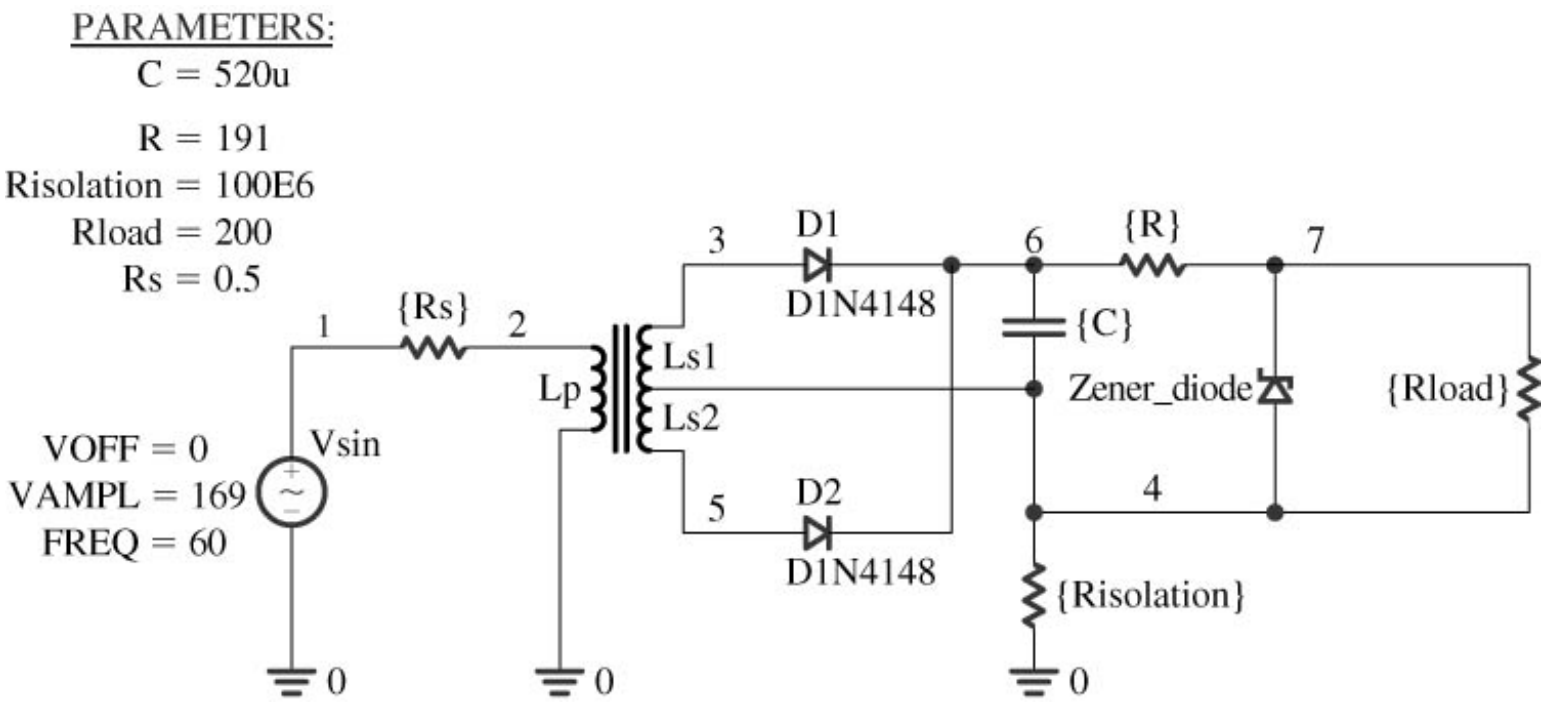


Figure 3.53 Capture schematic of the 5-V dc power supply in Example 3.10.

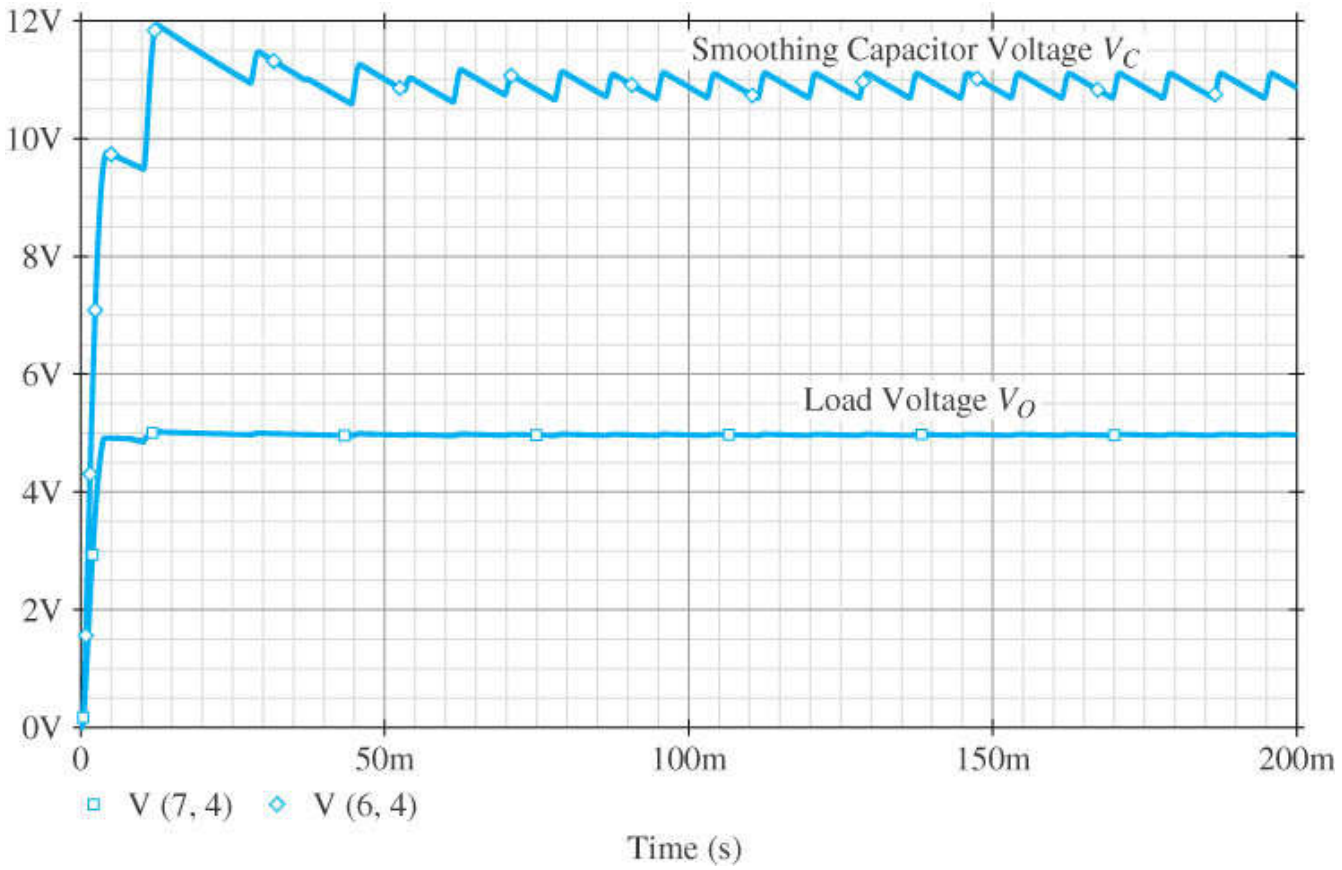


Figure 3.54 The voltage v_C across the smoothing capacitor C and the voltage v_O across the load resistor $R_{\text{load}} = 200\ \Omega$ in the 5-V power supply of Example 3.10.

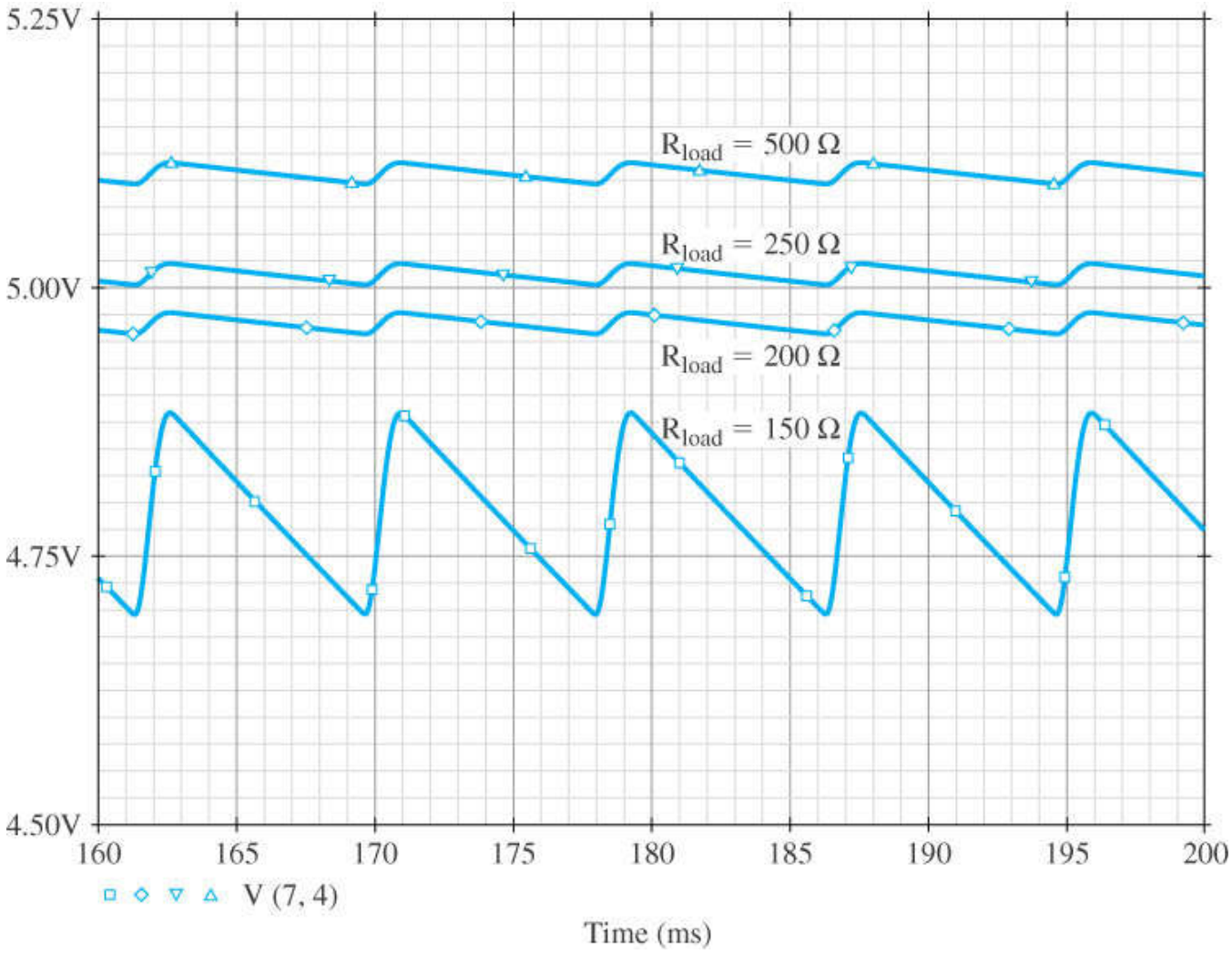


Figure 3.55 The output-voltage waveform from the 5-V power supply (in Example 3.10) for various load resistances: R_{load} = 500 Ω, 250 Ω, 200 Ω, and 150 Ω. The voltage regulation is lost at a load resistance of 150 Ω.

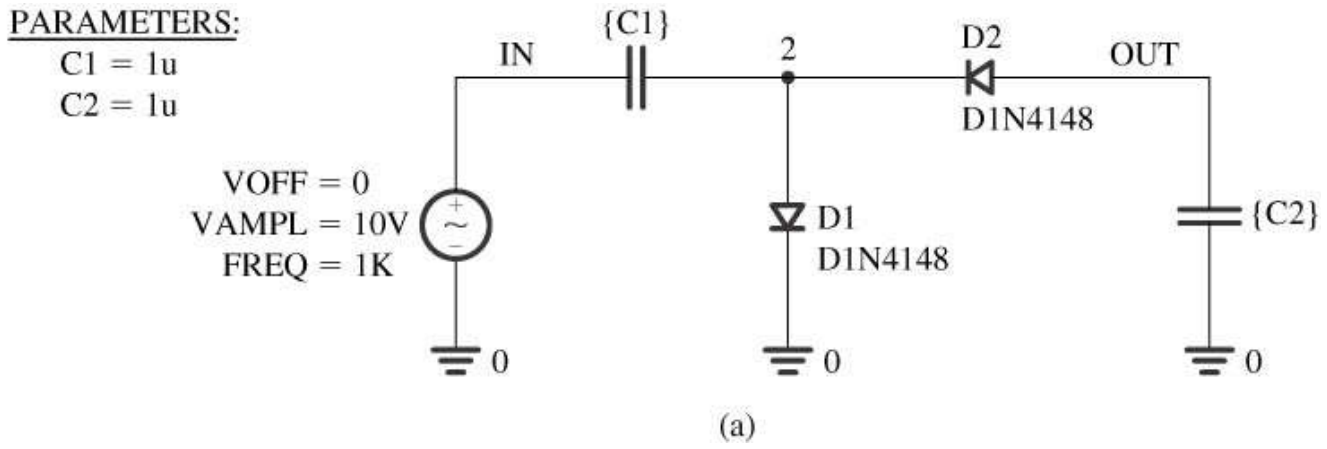


Figure E3.35 (a) Capture schematic of the voltage-doubler circuit (in Exercise 3.35).

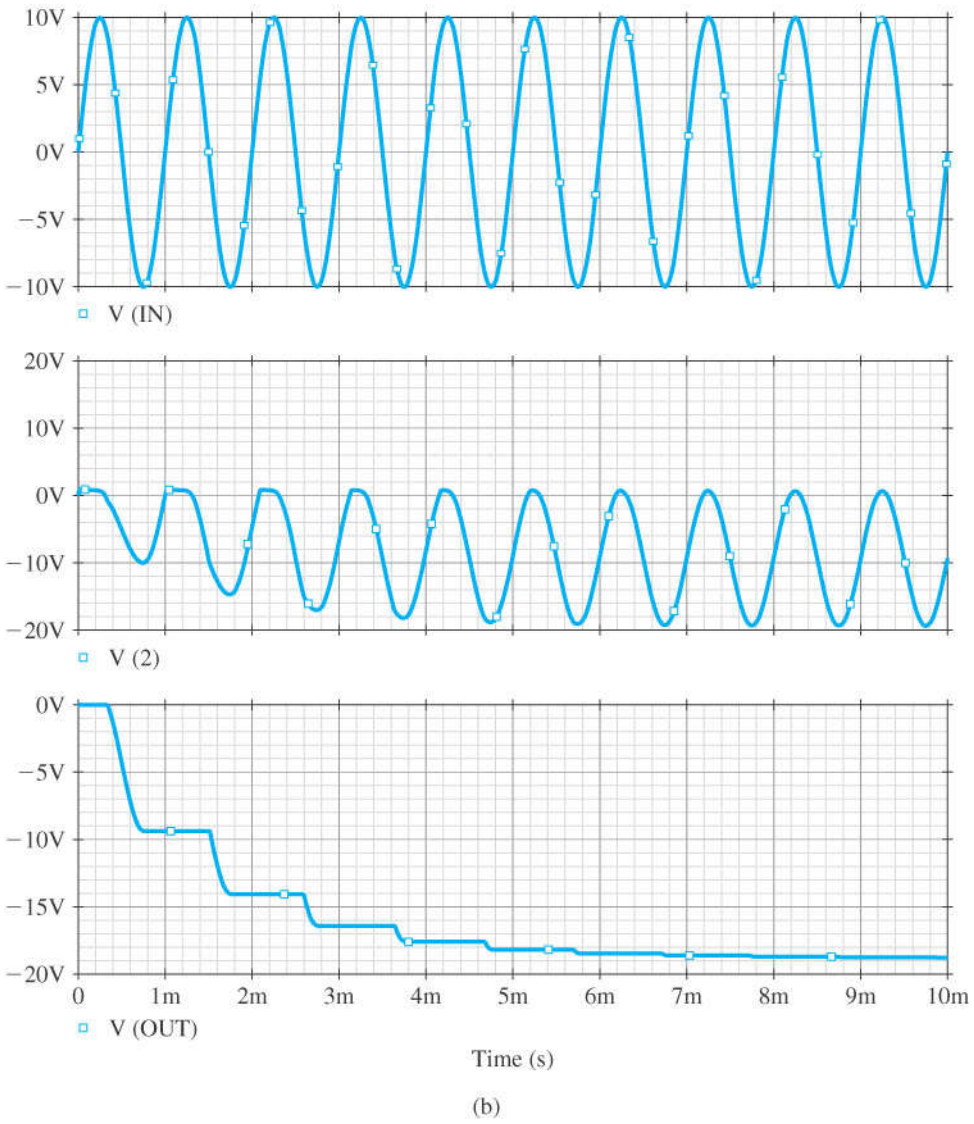


Figure E3.35 *(Continued)* **(b)** Various voltage waveforms in the voltage-doubler circuit. The top graph displays the input sine-wave voltage signal, the middle graph displays the voltage across diode D_1, and the bottom graph displays the voltage that appears at the output.

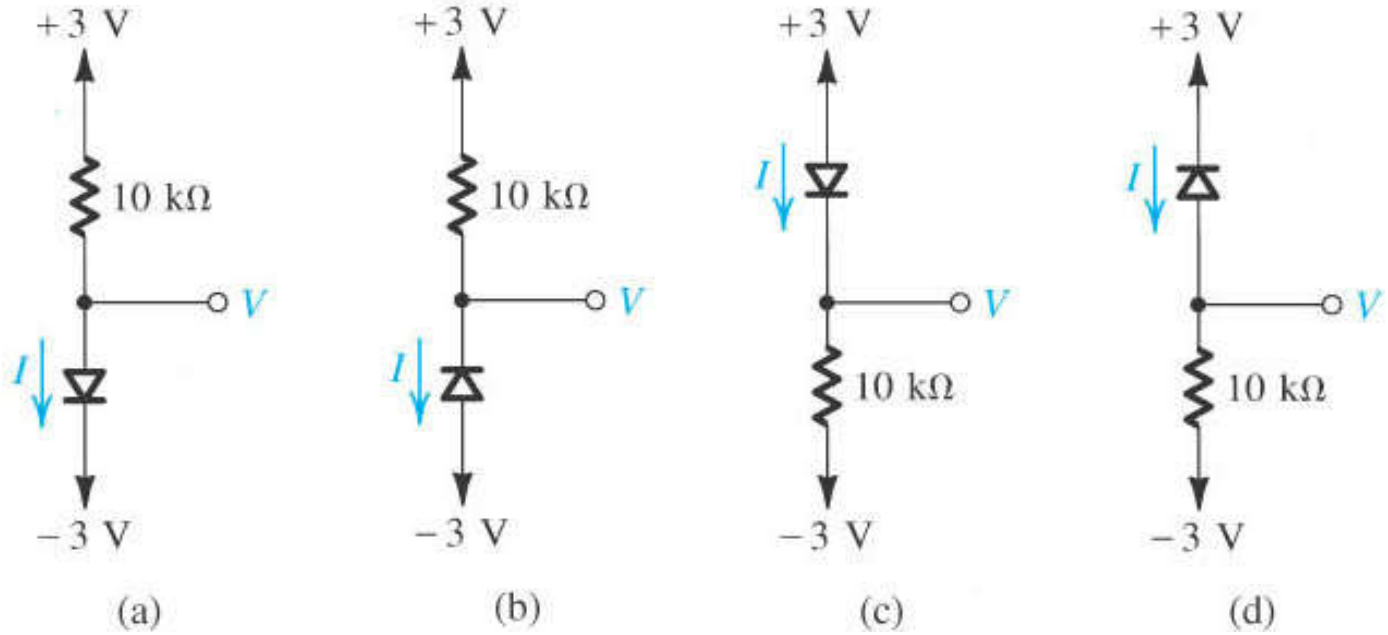


Figure P3.2

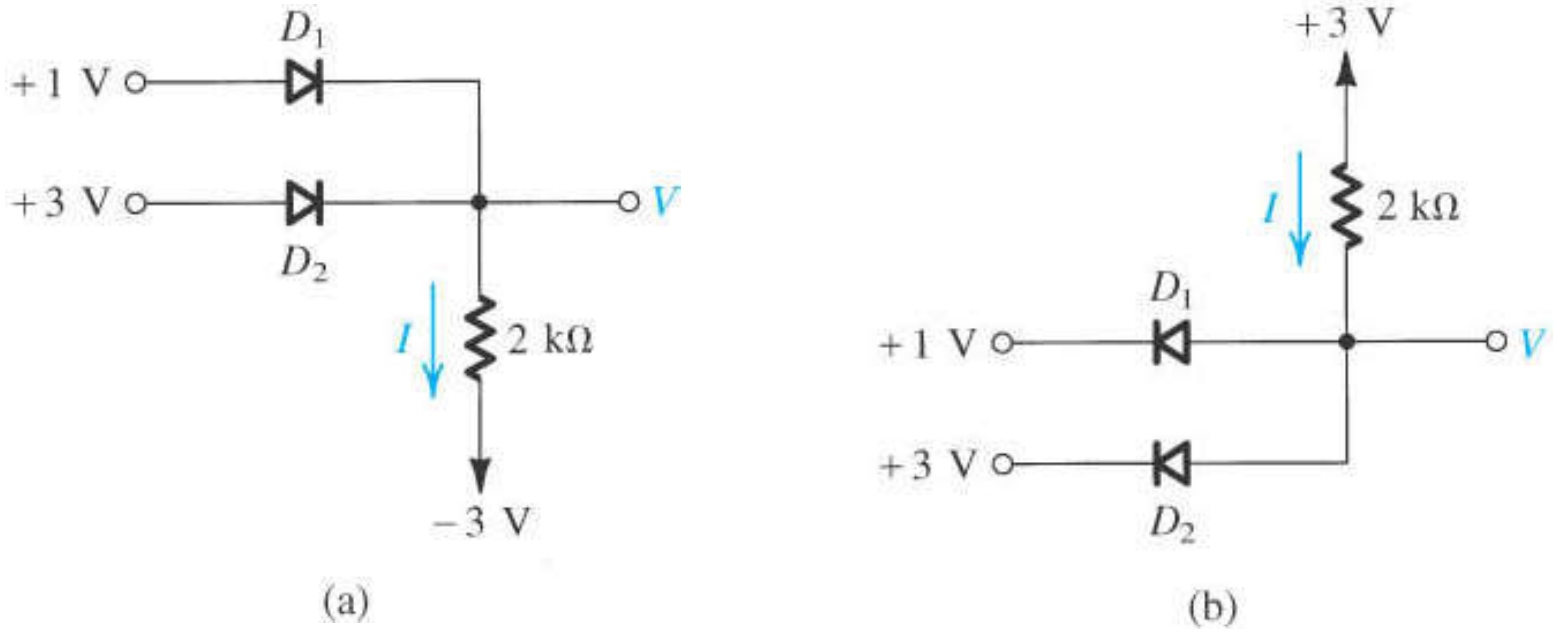


Figure P3.3

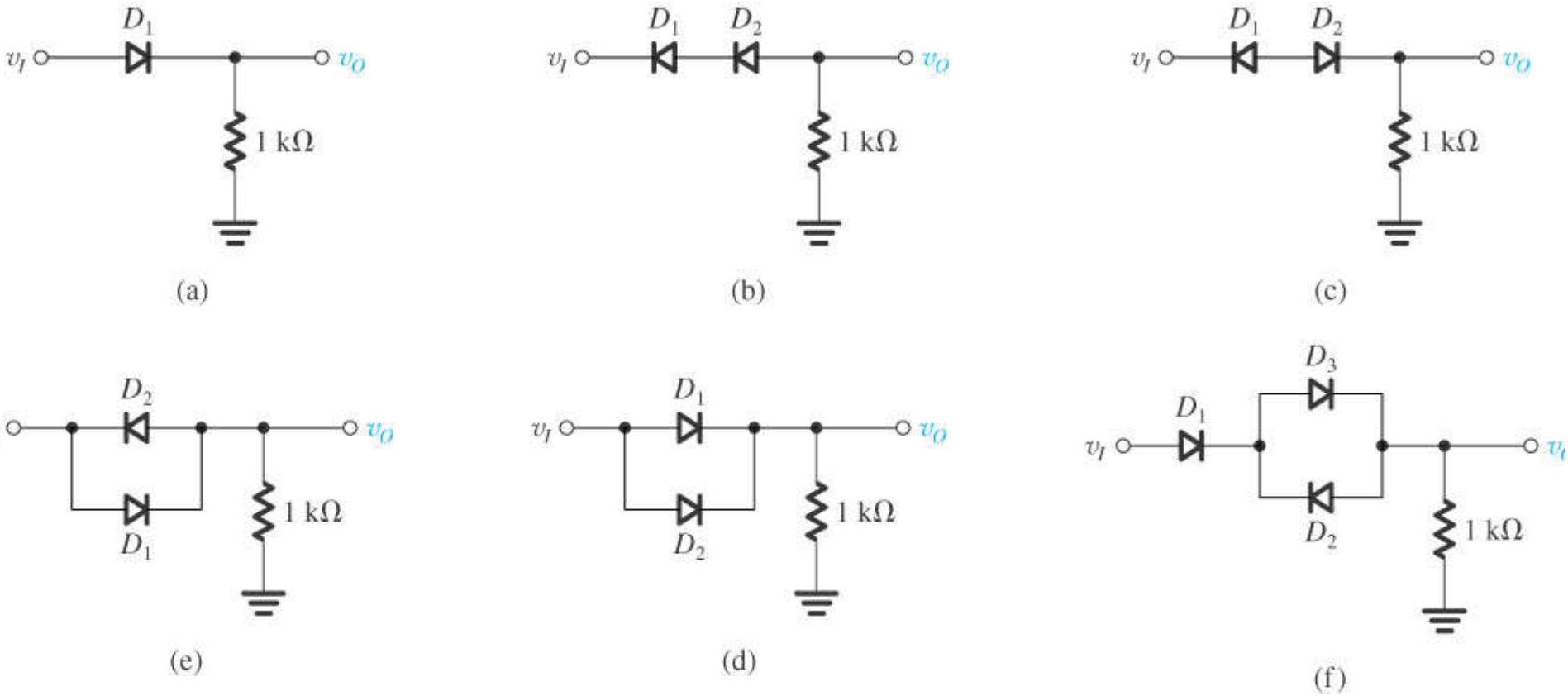
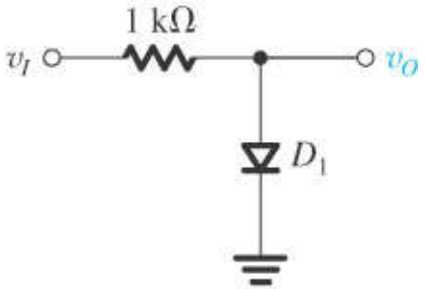
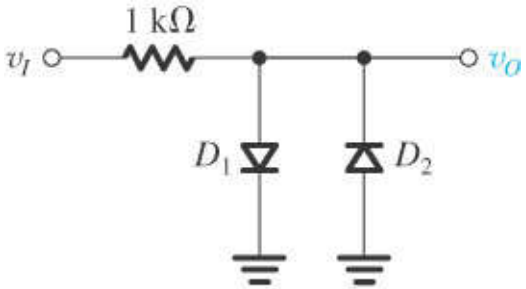


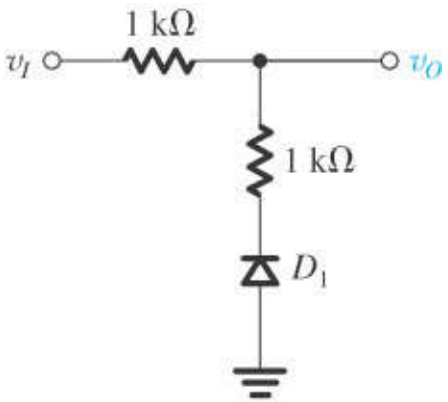
Figure P3.4 *(Continued)*



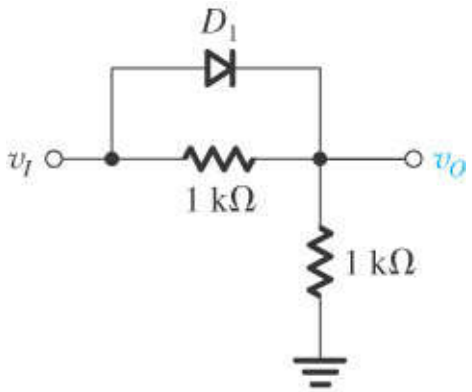
(g)



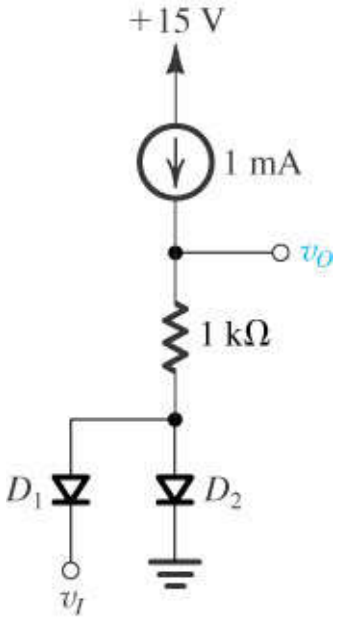
(h)



(i)



(j)



(k)

Figure P3.4 *(Continued)*

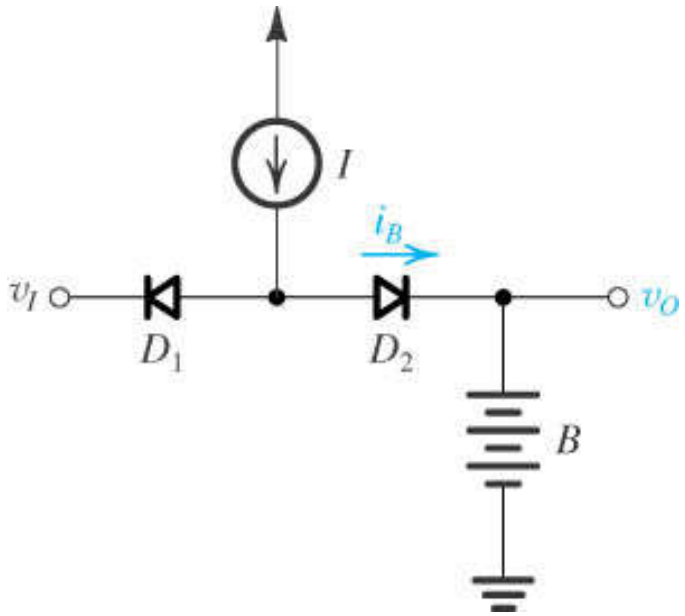


Figure P3.5

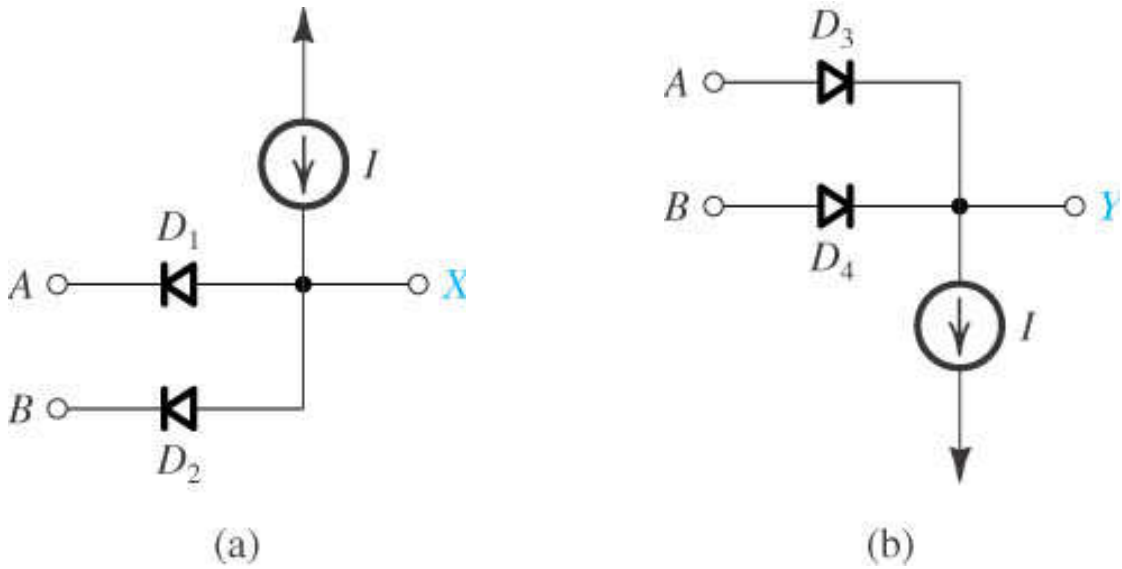


Figure P3.6

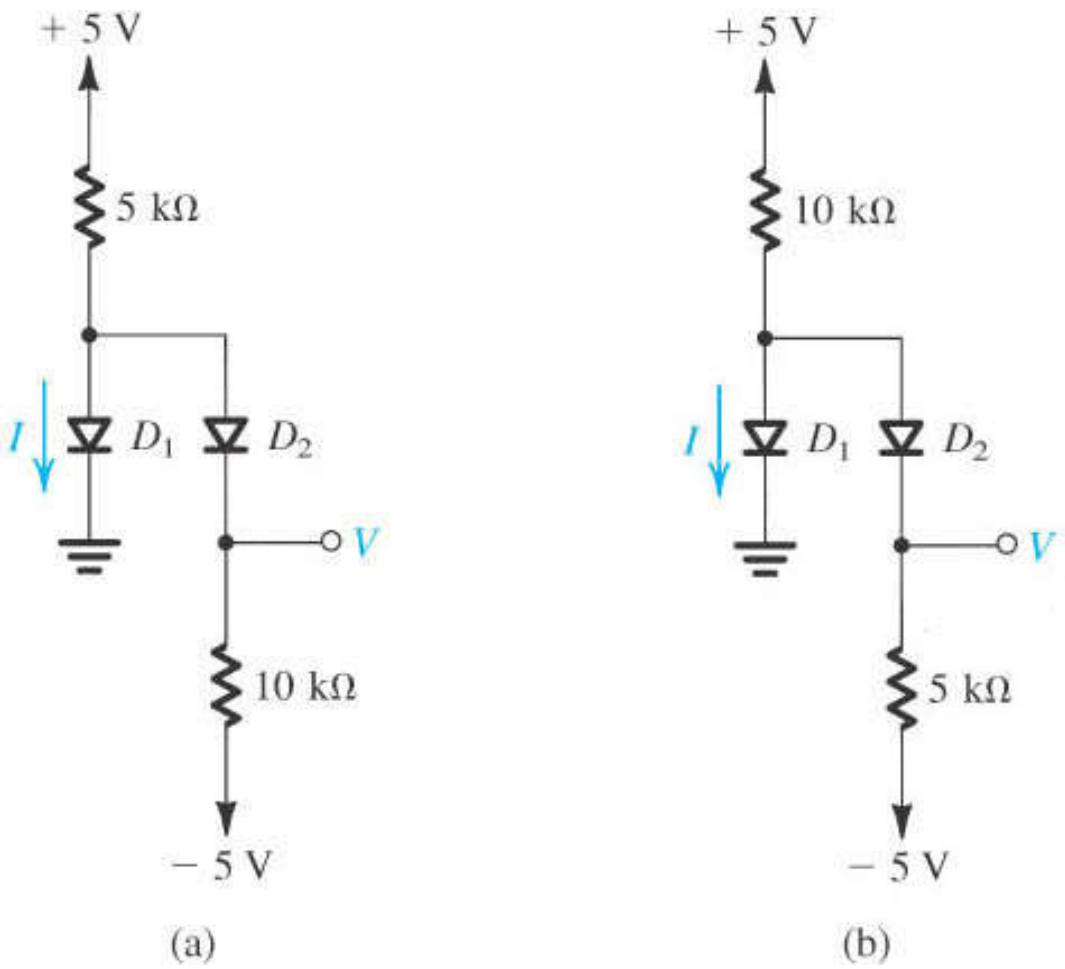


Figure P3.9

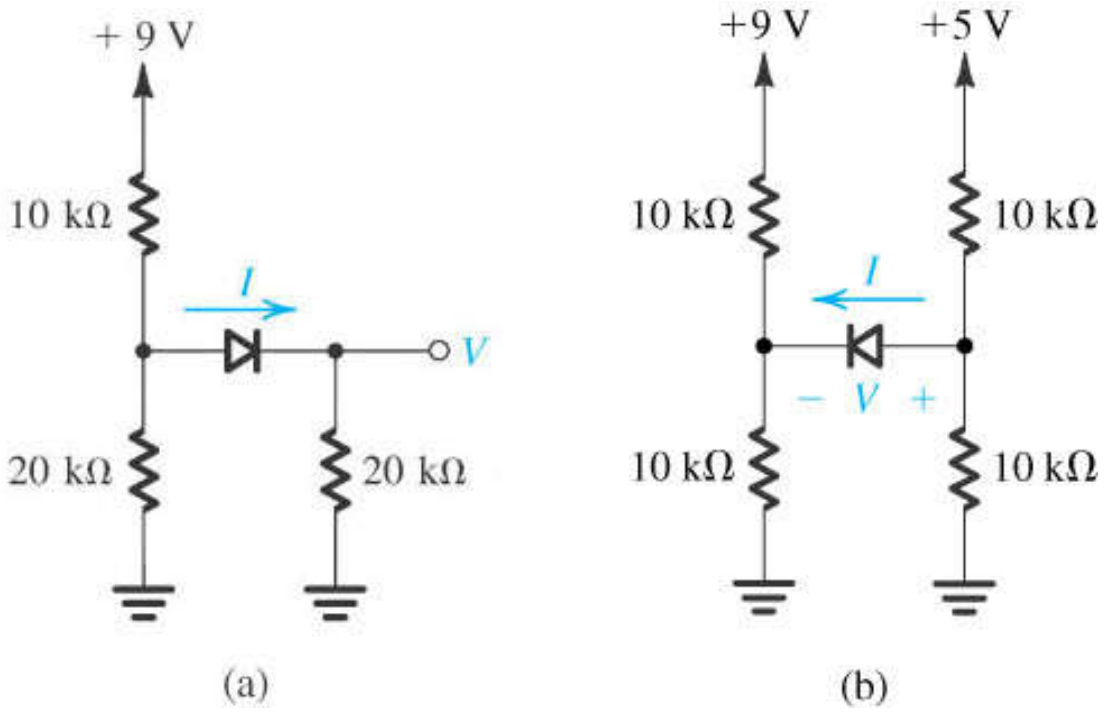


Figure P3.10

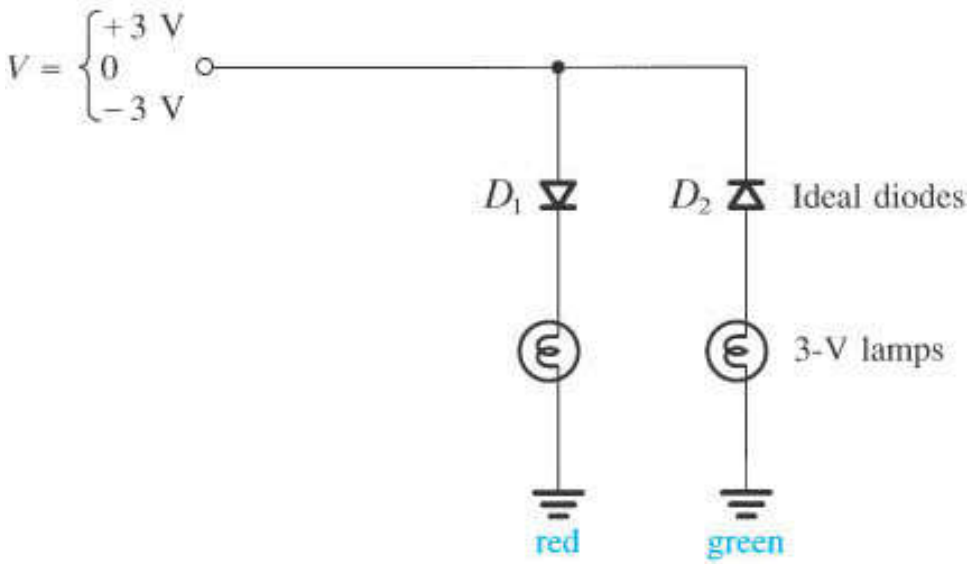


Figure P3.16

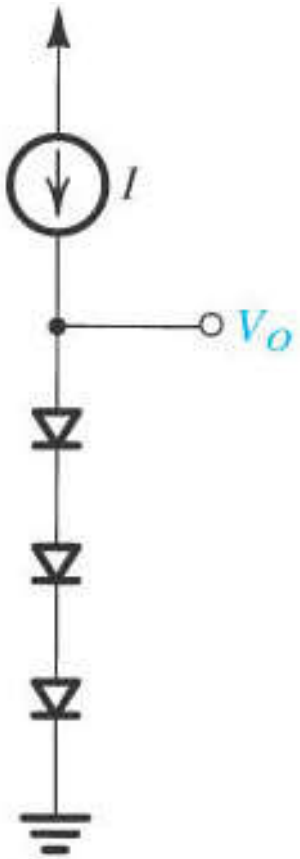


Figure P3.23

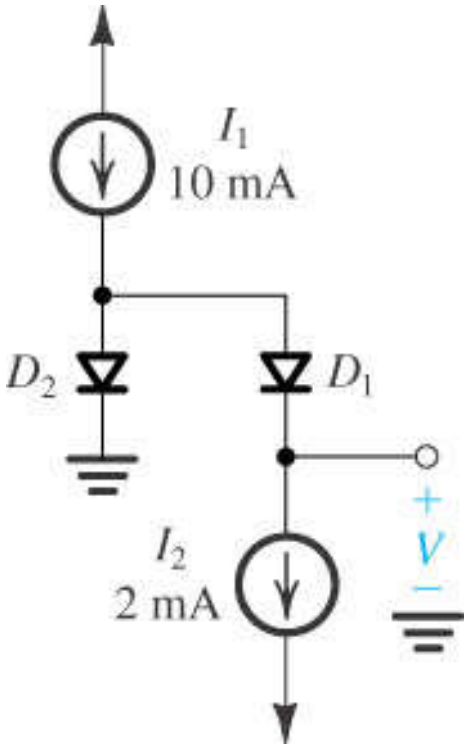


Figure P3.25

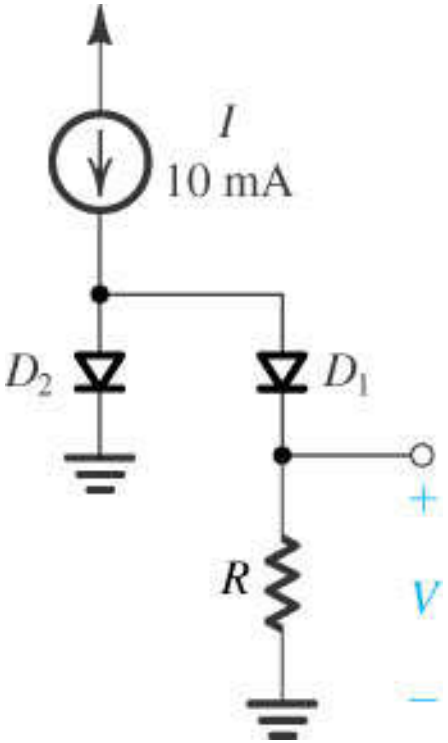


Figure P3.26

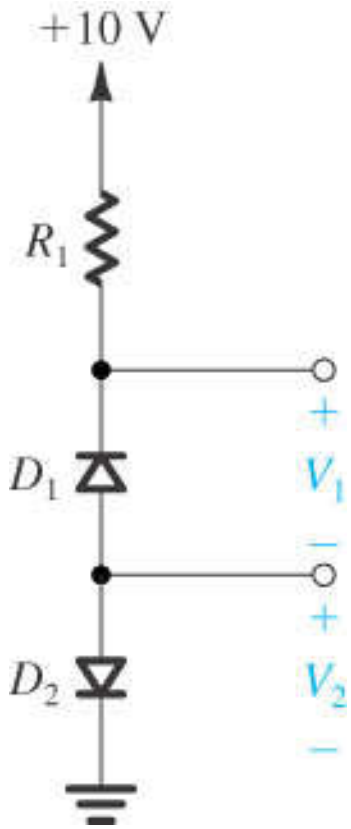


Figure P3.28

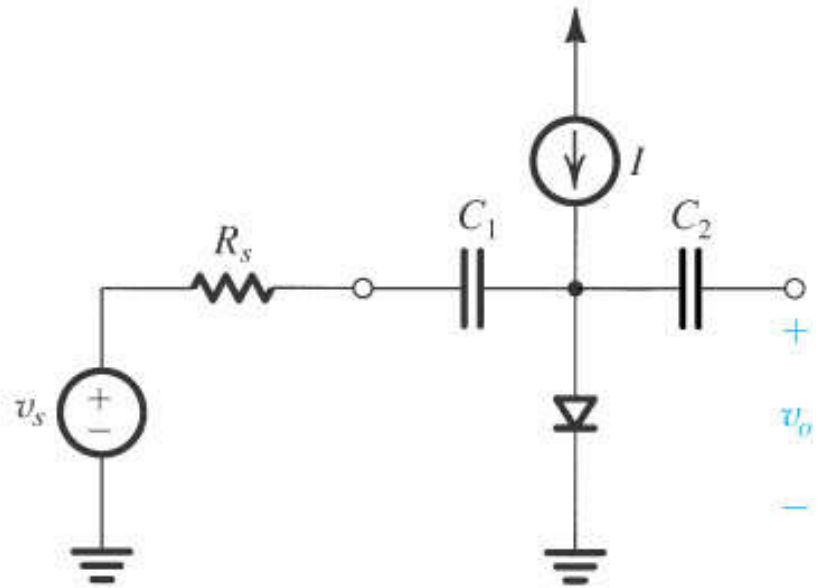


Figure P3.54

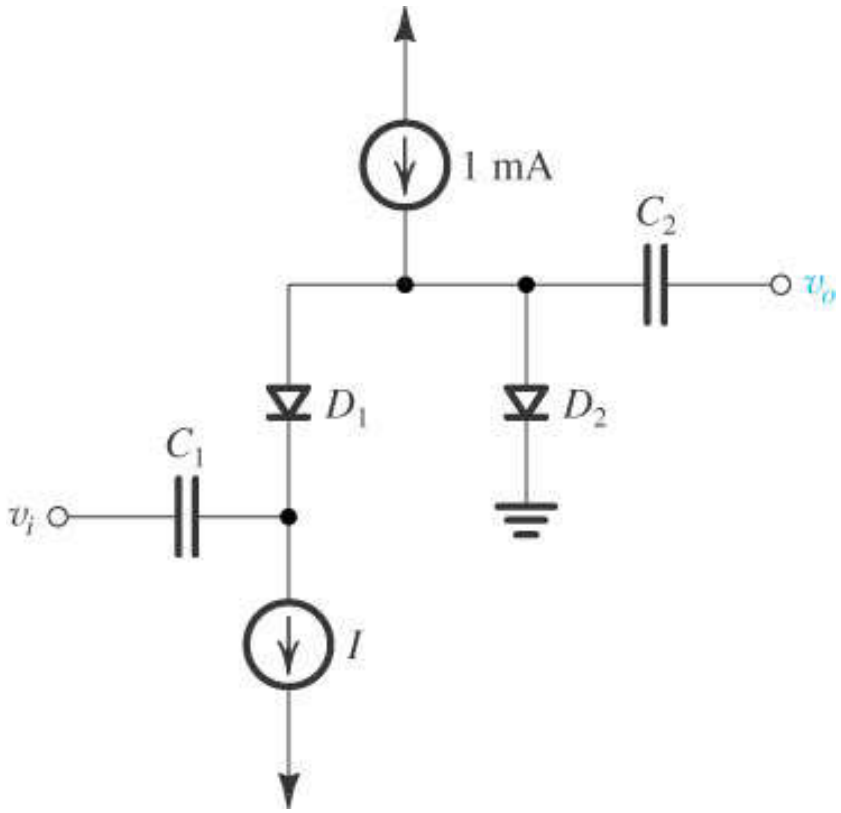


Figure P3.56

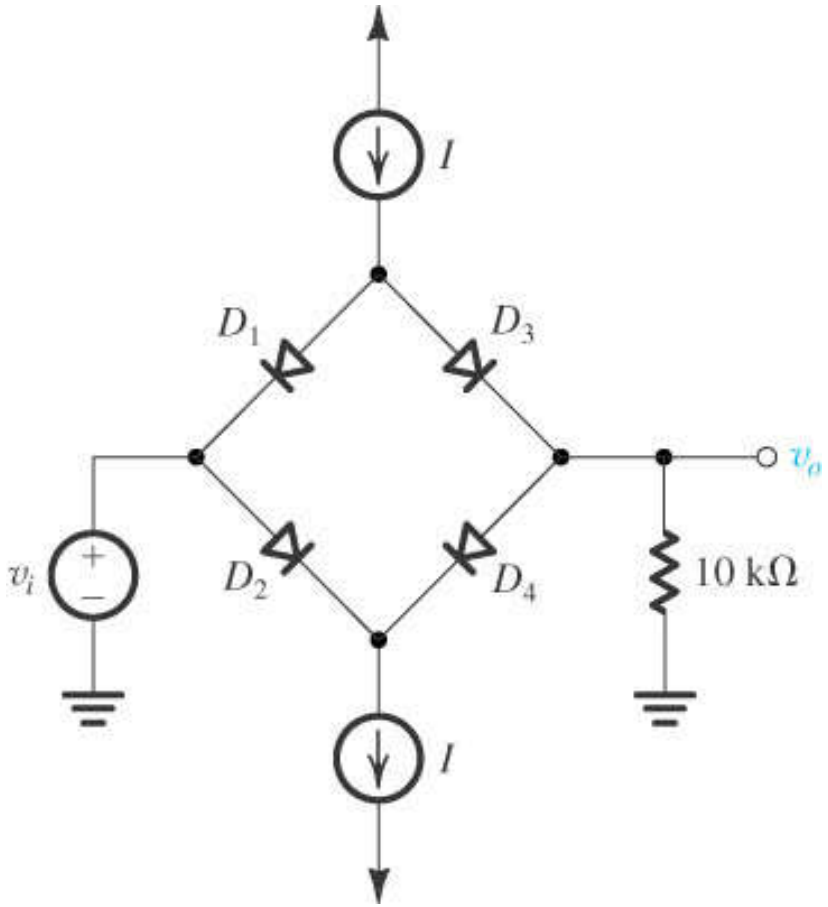


Figure P3.57

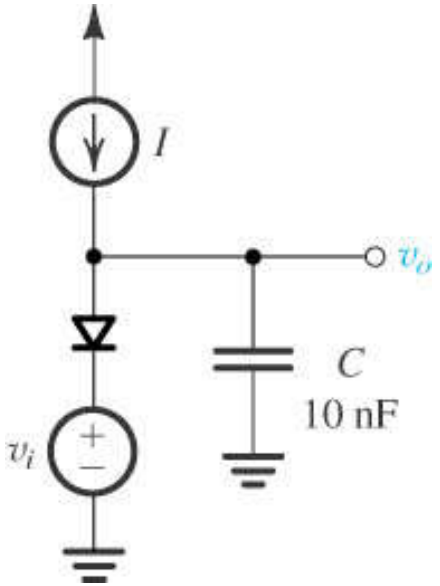


Figure P3.58

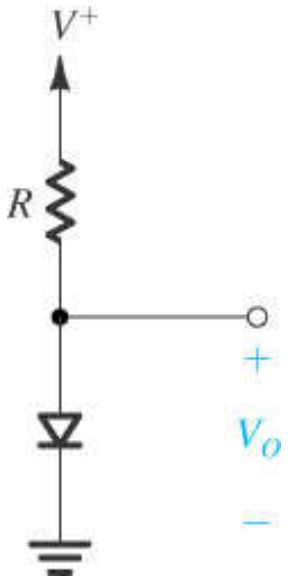


Figure P3.59

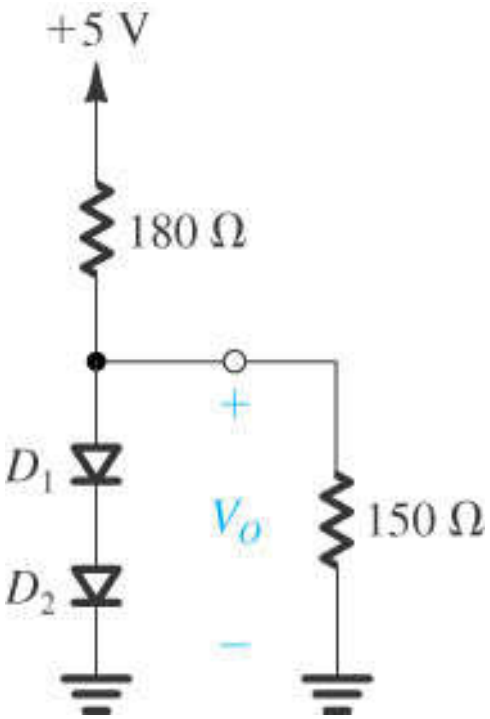


Figure P3.63

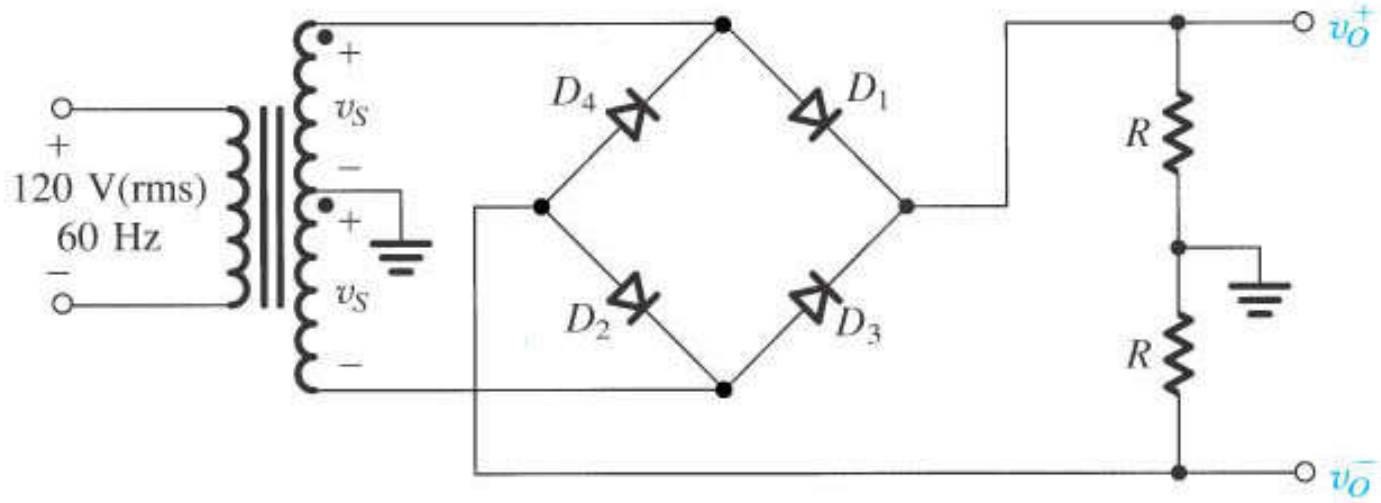


Figure P3.82

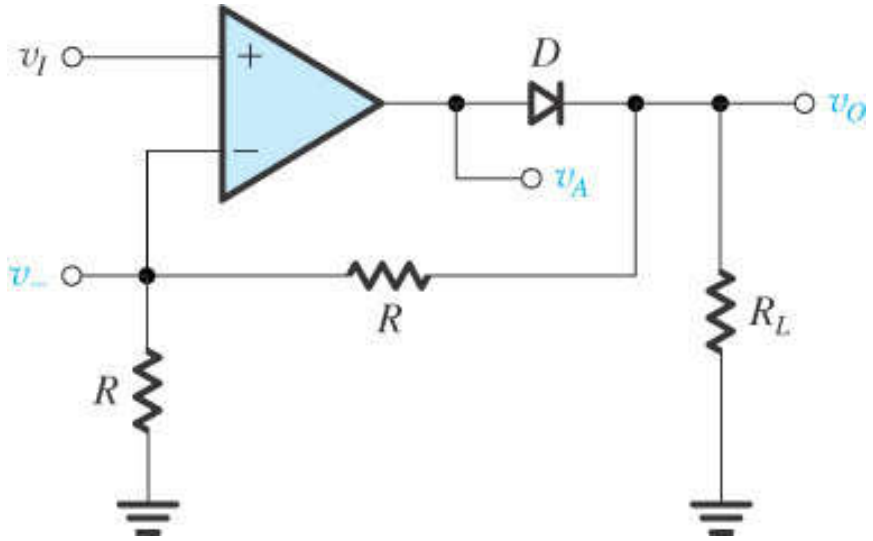


Figure P3.91

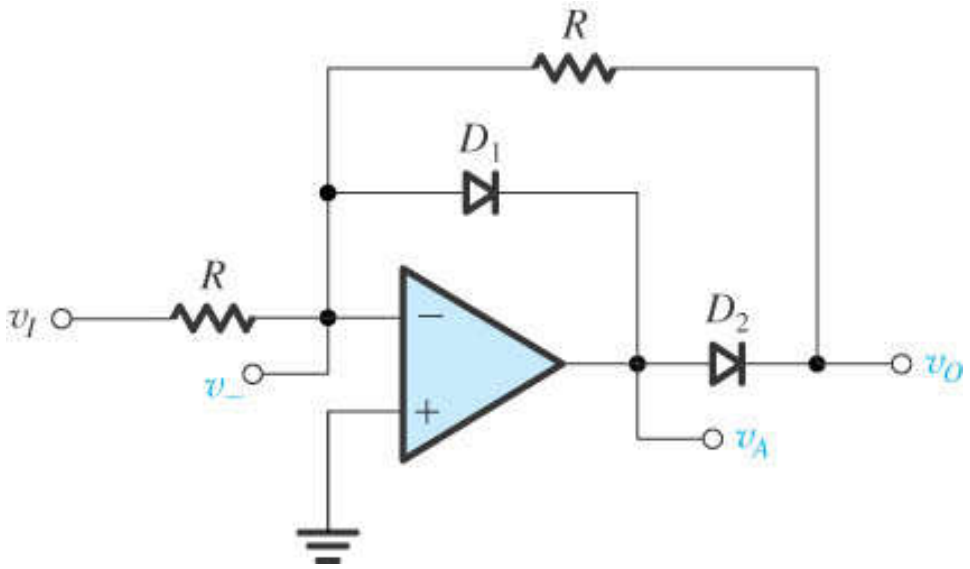


Figure P3.92

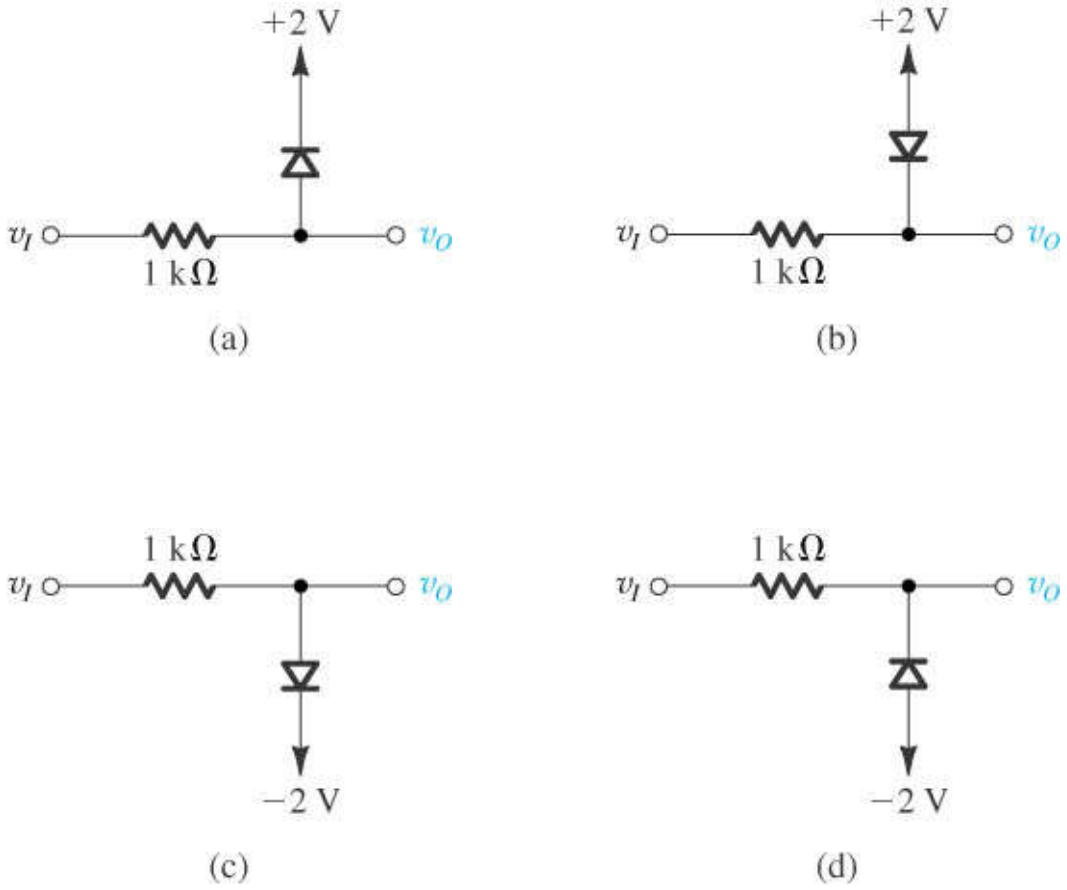


Figure P3.93

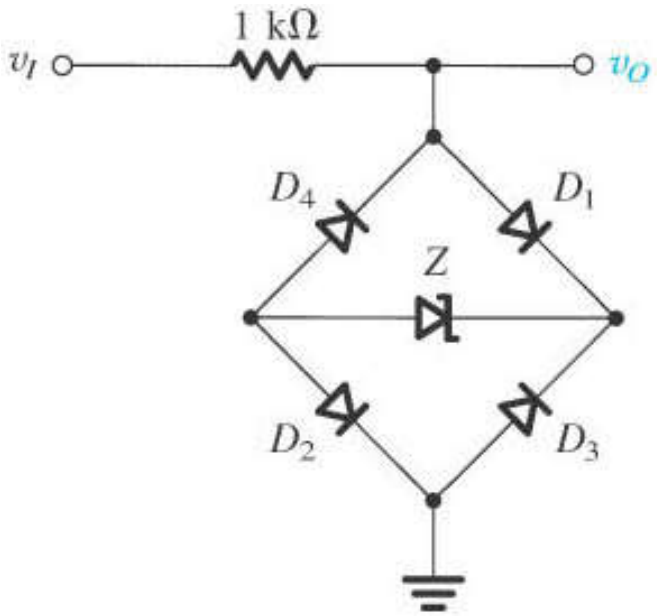


Figure P3.97

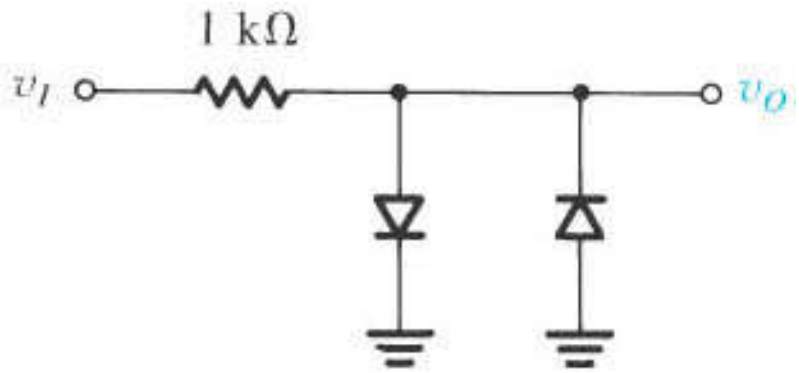


Figure P3.98

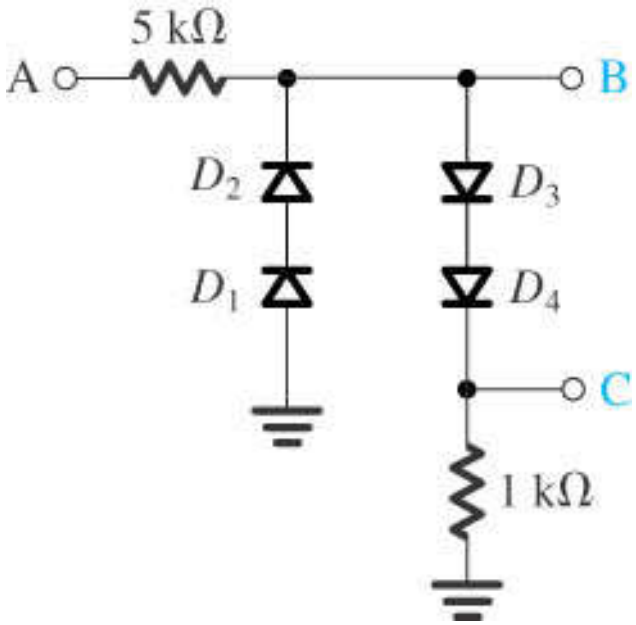


Figure P3.102

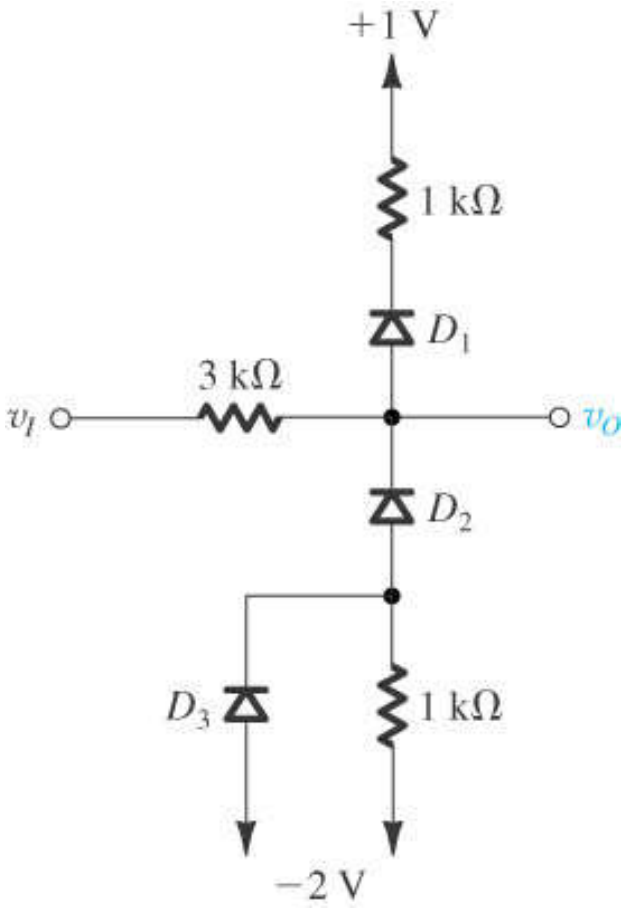


Figure P3.103

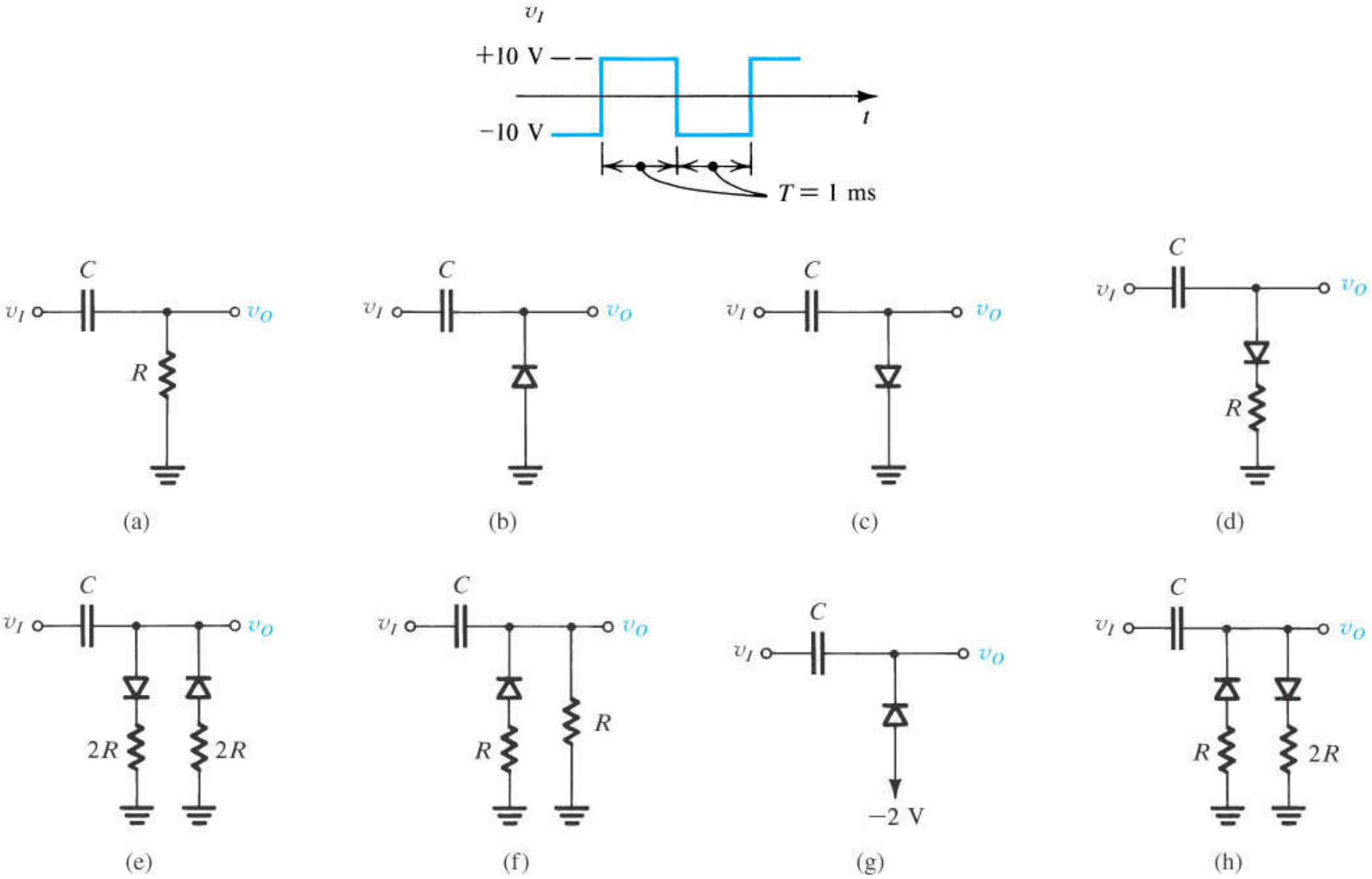


Figure P3.105

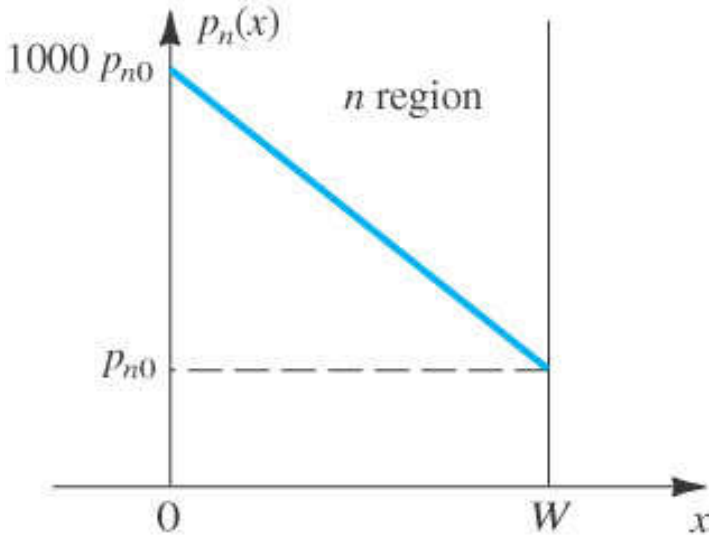


Figure P3.108