Analysis of Conduction in Fully Depleted SOI MOSFET's

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Abstract—**The conduction characteristics of fully depleted SOI MOSFET's have been studied by theoretical analysis and computer simulation. In these devices the ideal inverse subthreshold slope of 59.6 mV/decade will be obtained if the interface-state capacitances are much smaller than the gate-oxide capacitances. For above-threshold conduction, with decreasing silicon film thickness the inversion charges penetrate more deeply into the film and the transconductance increases because of the decreasing fraction of surface conduction.**

I. Introduction

MOSFET'S fabricated in fully depleted silicon-on-oxide (SOI) films have advantages over partially depleted SOI MOSFET's, because the fully depleted silicon film reduces the inverse subthreshold slope [1] and minimizes the floating-substrate and short-channel effects [2], [3]. Recently, Balestra *et al.* have reported simulation results showing strong transconductance enhancement in fully depleted SOI MOSFET's [4]. However, it was assumed that the substrate bias would be increased in proportion to the gate bias, a procedure that is not practical in actual circuit operation. Furthermore, no theoretical analysis was presented to assist in the design of such devices. In this paper, we propose a simple model for studying the conduction characteristics of fully depleted SOI MOSFET's. The calculated results, which have been verified by PISCES simulation [5], show a strong increase in transconductance without requiring the substrate bias to be varied with the gate bias.

II. One-Dimensional Model for SOI MOSFET's

A cross-sectional view of a fully depleted SOI MOSFET is shown in Fig. 1. If the device is operated before the onset of strong inversion—i.e., $\Phi(x) < 2\Phi_B$, where Φ_B is the potential difference between the extrinsic and intrinsic Fermi levels—the potential distribution through the film is given by a one-dimensional Poisson's equation [6], [7]

$$\frac{d^2\Phi(x)}{dx^2} = \frac{qN_A}{\epsilon_{Si}}, \qquad 0 \leq x \leq t_{Si} \tag{1}$$

where $\Phi(x)$ is the potential at a distance x below the top surface of the SOI film, N_A is the density of the ionized acceptors in the film, ϵ_{Si} is the dielectric constant of silicon, and t_{Si} is the silicon film thickness.

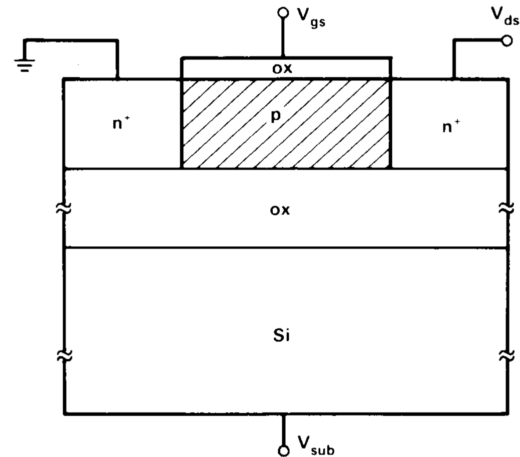

Fig. 1. Cross-sectional view of an n-channel fully depleted SOI MOSFET. The shaded region denotes the depletion region.

For fully depleted SOI MOSFET's, the boundary conditions for (1) are

$$\Phi(0) = \Phi_f \tag{2}$$

$$\left.\frac{d\Phi(x)}{dx}\right|_{x=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f - V'_{gs}}{t_f} \tag{3}$$

$$\Phi(t_{Si}) = \Phi_b \tag{4}$$

$$\left.\frac{d\Phi(x)}{dx}\right|_{x=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{V'_{sub} - \Phi_b}{t_b} \tag{5}$$

with

$$V'_{gs} = V_{gs} - V_{FB,f} \tag{6}$$

$$V'_{sub} = V_{sub} - V_{FB,b} \tag{7}$$

where Φ_f is the potential at the front-side oxide–silicon interface, ϵ_{ox} is the dielectric constant of SiO_2, V_{gs} is the gate-source bias voltage, $V_{FB,f}$ is the front-channel flat-band voltage, t_f is the front-gate-oxide thickness, Φ_b is the potential at the back-side silicon–oxide interface, V_{sub} is the substrate-source bias voltage, $V_{FB,b}$ is the back-channel flat-band voltage, and t_b is the buried-oxide thickness.

We assume that the buried-oxide capacitance, C_b =

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ϵ_{ox}/t_b, is much smaller than the front-gate-oxide capacitance, $C_f = \epsilon_{ox}/t_f$, and the silicon-film capacitance, $C_{Si} = \epsilon_{Si}/t_{Si}$. Solving (1) under boundary condition (2)–(5) then gives

$$\Phi(x) = \frac{qN_A x^2}{2\epsilon_{Si}} + \left(-\frac{qN_A t_{Si}}{\epsilon_{Si}} + \frac{C_b V'_{sub}}{\epsilon_{Si}}\right)x + \Phi_f \quad (8)$$

with

$$\Phi_f = -\frac{qN_A t_{Si}}{C_f} + V'_{gs} + \frac{C_b}{C_f} V'_{sub}$$

$$\Phi_b = -\frac{qN_A t_{Si}}{C_f}\left(1 + \frac{C_f}{2C_{Si}}\right) + V'_{gs} + \left(\frac{C_b}{C_f} + \frac{C_b}{C_{Si}}\right)V'_{sub}. \quad (10)$$

To verify the proposed analytical model, the PISCES program was used to simulate the potential distribution within the silicon film. Fig. 2 plots the calculated and simulated values of Φ_f and Φ_b as functions of V_{gs}. Before strong inversion occurs, the data calculated from the model agree with the PISCES simulation results. When V_{gs} is increased sufficiently to cause strong inversion near the front channel, the high-density inversion charge near the front channel shields the back channel from the front-gate bias, so that Φ_b becomes insensitive to V_{gs}.

III. Subthreshold Characteristics

The subthreshold current is the sum of the front-channel current $I_{ds,f}$ and the back-channel current $I_{ds,b}$. In either channel, the subthreshold current is given approximately by [6]

$$I_{ds,i} = \delta_i\left[1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right] \cdot \left[\exp\left(\frac{\Phi_i}{V_T}\right)\right]\left(\frac{\Phi_i}{V_T}\right)^{-1/2}, \quad i = f, b \quad (11)$$

where δ_i is a device-dependent parameter, V_{ds} is the drain–source voltage, and V_T is the thermal voltage.

The inverse subthreshold slope, which is defined as $S \equiv \ln(10)\, dV_{gs}/d \ln I_{ds}$, can be calculated from (9)–(11) as

$$S = \ln(10) V_T \left[\frac{1}{1 + \frac{C_{it,f}}{C_f}} \frac{I_{ds,f}}{I_{ds}} + \frac{1}{1 + \frac{C_{it,b}}{C_f} + \frac{C_{it,b}}{C_{Si}}} \frac{I_{ds,b}}{I_{ds}}\right]^{-1} \quad (12)$$

where $C_{it,f} = qD_{it,f}$ and $C_{it,b} = qD_{it,b}$ are the interface-state capacitances corresponding to $dV_{FB,f}/dV_{gs}$ and $dV_{FB,b}/dV_{gs}$, respectively, and $D_{it,f}$ and $D_{it,b}$ are the interface-state densities.

For practical device operation, the back-channel current is generally suppressed to prevent leakage. In this

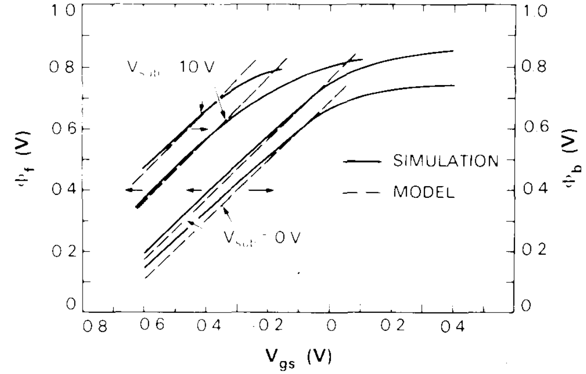

Fig. 2. Comparison of calculated channel potentials Φ_f and Φ_b (dashed source bias voltage V_{gs} for two values of substrate-source bias voltage V_{sub}.

case, (12) can be rewritten as

$$S = \ln(10) V_T \left[1 + \frac{C_{it,f}}{C_f}\right]. \quad (13)$$

As indicated by (13), the inverse subthreshold slopes of fully depleted SOI MOSFET's do not include the depletion capacitance term and can therefore be much lower than those of bulk-silicon and partially depleted SOI devices. When the ratio $C_{it,f}/C_f$ is small enough, S reaches the ideal value of $\ln(10) V_T = 59.6$ mV/decade, independent of t_f, t_{Si}, and N_A.

IV. Transconductance

It has been observed [8], [9] that thin (800 Å) fully depleted SOI MOSFET's can have up to 50 percent higher transconductance than their thick (2000 Å) counter-parts. The thin-film-induced transconductance enhancement can be explained by the effects of the electric field and inversion charge distribution on the electron mobility in the SOI films. From (8), the vertical electric field before strong inversion is given by

$$E_x(x) = -\frac{d\Phi}{dx} = \frac{qN_A(t_{Si} - x)}{\epsilon_{Si}} - \frac{C_b V'_{sub}}{\epsilon_{Si}}. \quad (14)$$

For fixed V'_{sub}, at a given depth E_x decreases as t_{Si} decreases. In Figs. 3 and 4 the vertical electric field and concentration of inversion charge, respectively, are plotted against depth for two devices with t_{Si} = 500 and 2000 Å. The fraction of surface charge also decreases with decreasing t_{Si}. For the device with the thicker film, surface conduction dominates, but body conduction makes an important contribution for the thinner device. The effective carrier mobility is lower for the thicker device because 1) as a result of surface scattering, surface mobility is lower than body mobility for the same electric field, and 2) the field-induced reduction in mobility is greater in the surface region, where the field is higher. The effect of surface scattering is illustrated in Fig. 5, where the simulated effective mobility μ_{eff} is plotted as a function of t_{Si} for fully depleted devices with different values of the electron

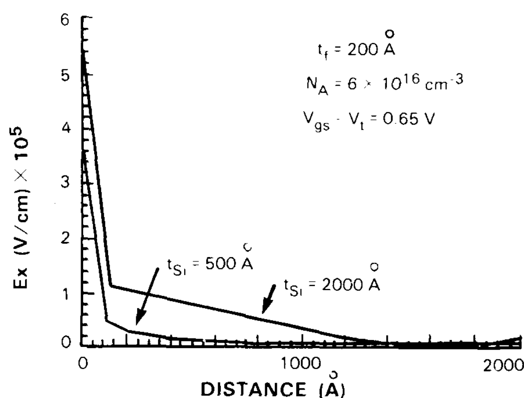

Fig. 3. Vertical electric field versus distance from surface for silicon films with t_{Si} = 500 and 2000 Å.

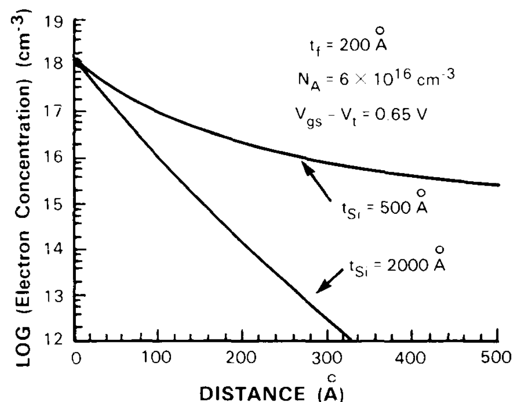

Fig. 4. Inversion charge concentration versus distance from surface for silicon films with t_{Si} = 500 and 2000 Å.

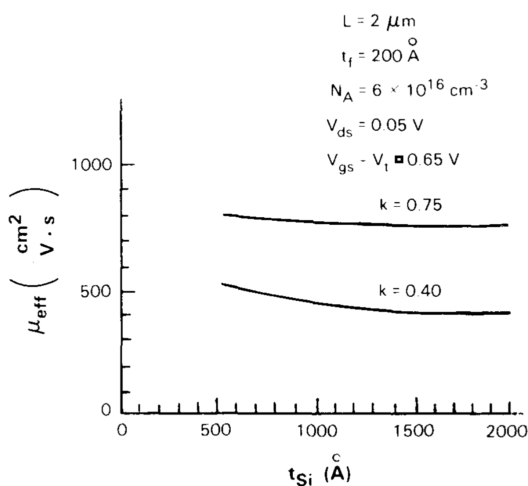

Fig. 5. Dependence of effective mobility μ_{eff} on t_{Si} for different values of the electron mobility degradation factor k.

mobility degradation factor k, defined as the ratio of surface mobility to body mobility. For $k < 1$, μ_{eff} increases with decreasing t_{Si}, causing the transconductance to increase. The dependence of μ_{eff} on t_{Si} is more pronounced for smaller k. (In Fig. 5 the effect of the electric field on mobility has been neglected, since the PISCES model for this effect is oversimplified.)

V. Conclusion

The conduction characteristics of fully depleted SOI MOSFET's have been studied by a simple analytical model and PISCES simulation. If $C_{it,f}$ is much smaller than C_f, S reaches the ideal value of ln (10) V_T, independent of t_f, t_{Si}, and N_A. Decreasing the SOI film thickness causes a reduction in the concentration of inversion charge in the vicinity of the film surface, which causes the transconductance to increase.

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